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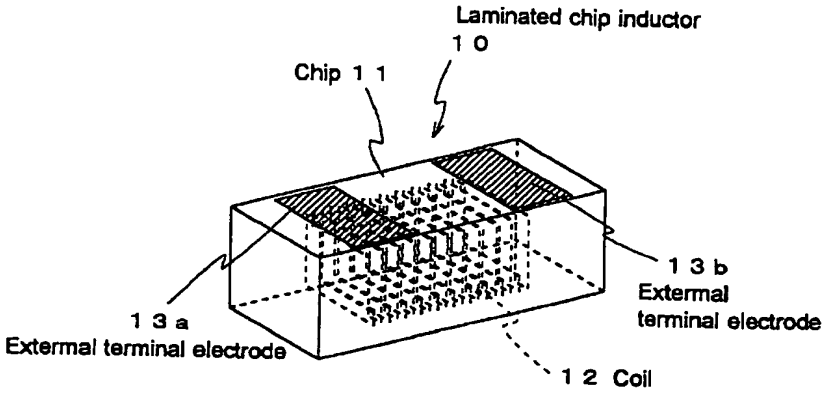
(54) Multi-laminated inductor and manufacturing method thereof

(57) A multi-laminated chip inductor (10) comprising a chip (11) provided therein with a coil (12) made by laminating insulating material sheets having internal conductors (21a) formed thereon and connecting the internal conductors (21a) into a helical shape and with lead internal conductors (22a through 25a) making connection between ends of the coil (12) and external terminal electrodes, and having external terminal electrodes (13a and 13b) formed on the surface of the chip (11) parallel to the winding center-line of the coil (12). Thereby, as the magnetic flux generated by the coil (12) does not intersect the plane of the external terminal electrodes (13a, 13b), eddy current within the external terminal electrodes (13a, 13b) can be prevented from generating and, the inductance values can be changed easily, by changing the connection position of the lead internal conductors (22a through 25a) with a coil end.

Fig. 1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a multi-laminated inductor used for various circuits and a manufacturing method and more particularly to a multi-laminated inductor comprised of laminated internal conductors forming a coil along the length of the chip.

Description of the Related Art

[0002] Conventional multi-laminated inductors are classified into two broad categories in the relation between the direction of laminating internal conductors and the outside shape of the chip, which form the coil. For example, multi-laminated chip inductors have such a structure that coil-shaped internal conductors made of silver or silver-palladium alloy are contained in a non-conductor material or ferrite magnetic material and both ends of the coil are connected to external terminal conductors respectively.

[0003] FIG. 2 shows a relation between the direction of laminating internal conductors and the outside shape of the chip in this multi-laminated chip inductors. It has one structure that the internal conductors 2 are laminated along the thickness Lt (or width Lw) of the multi-laminated chip inductor 1. Usual multi-laminated chip inductors have this structure. Here, the both ends of a coil-shaped conductor are connected to external terminal conductors 3a and 3b, respectively.

[0004] On the other hand, Japanese Patent Application Laid-Open No. 8-55726 teaches the another structure of a multi-laminated chip inductor 6 as shown in FIG. 3. That is, internal conductors 4 are laminated along the length L1 of the chip 6 and are external terminal conductors 5a and 5b formed at both end portions along its length.

[0005] This structure is generally referred to as a longitudinal stack type, and has features that it can provide relatively high inductance values and high self-resonance frequencies.

[0006] A multi-laminated chip inductor of the longitudinal stack type has a laminated structure as shown in FIG. 4, for example. That is, a coil is formed by laminating a plurality of magnetic material sheets 7a and 7b having internal conductor patterns 4a and 4b shaped like a letter L thereon, and then connecting the internal conductors 4a and 4b through via holes 8a and 8b into the shape of a spiral. Further, both ends of the coil formed by the internal conductor patterns 4a and 4b are connected to via holes 8c and 8d formed in a plurality of laminated magnetic material sheets 7c and 7d, respectively.

[0007] Thereby, lead conductor portions are formed by coupling a plurality of via holes 8c and 8d. The via holes 8c and 8d exposed to the surfaces of the magnetic material sheets 7c and 7d placed at both ends are connected to the external terminal electrodes 5a and 5b. These external terminal conductors 5a and 5b are formed on the both end faces along the length of the chip and on portions of the faces adjacent to these end faces.

[0008] In the conventional multi-laminated chip inductors 6 of the longitudinal stack type described above, the external terminal electrodes 5a and 5b are formed on both end faces along the chip length in which are perpendicular to the winding center-line of the coil formed by internal conductors 4.

[0009] Therefore, when the magnetic flux generated by the passage of electric current through the coil passes through the external terminal electrodes 5a and 5b, eddy current is generated within the external terminal electrodes 5a and 5b. This eddy current has been one of the factors that increase its electrical loss.

[0010] Further, as the internal conductors 4 and the external terminal electrodes 5a and 5b are disposed nearly parallel to each other, stray capacity is produced between them. This stray capacity has been one of the factors behind a reduction in the self-resonance frequency of the inductors.

[0011] Also, in manufacturing of multi-laminated chip inductors of the longitudinal stack type described above, there has been no approach for adjusting a value of inductance except re-designs such as changing the core area. It has been also necessary to change the content of design for each different value of inductance. Thus, the control of design specification has been very complex.

BRIEF SUMMARY OF THE INVENTION

[0012] Considering the problems described above, it is an objection of the present invention to provide a multi-laminated inductor and a method for manufacturing it which allow reducing eddy current generated within an external terminal electrode and further an easy adjustment/modification of a value of inductance.

[0013] In order to achieve the objective described above, by providing a lead layer having a lead internal conductor exposed to a chip surface nearly parallel to the winding center-line of a coil and connected to an end of the coil for a predetermined layer, and forming an external terminal electrode formed on a face nearly parallel to the winding center-line of the coil and connected to the lead internal conductor, a multi-laminated inductor having the chip with a laminated structure having the coil buried therein and the external terminal electrode formed on the chip surface and connected to the coil is configured.

[0014] According to this multi-laminated inductor, the external terminal electrodes are formed on the faces parallel to the winding center-line of a coil, so that the magnetic flux generated by the passage of electric cur-

rent through the coil does not intersect the external terminal electrodes surface. Thus, eddy current within the external terminal electrodes is prevented from generating, and so increasing the loss generated by the eddy current can be suppressed.

[0015] Also, by providing a lead internal conductor exposed to all the faces parallel to the winding center-line of a coil, it is not necessary to select a face having the external terminal electrode exposed therein at the production of the coil, so that the manufacturing process can be simplified.

[0016] Also, according to the invention, the multi-laminated inductor described above is provided with a chip shaped like a rectangular solid which has square-shaped insulating material sheets laminated therein and further provided with a lead layer comprising an insulating material sheet having a first lead internal conductor formed thereon and an insulating sheet having a second lead internal conductor formed thereon; wherein the first lead internal conductor is formed like a cross shape with a predetermined width and has its intersection point at the center of the insulating material sheet and their four edges reach to the four edges of the insulating material, and the second lead internal conductor is formed like a linear shape with a predetermined width and placed so that one end thereof is connected to the first lead internal conductor nearly at the center of the insulating material sheet and the other end thereof is connected to a predetermined spot of the end of the coil.

[0017] According to this multi-laminated inductor, the coil and the external terminal electrode are electrically connected by means of the first and second lead internal conductors. Since these first and second lead conductors are formed like a cross and linear shape respectively, the area intersecting the magnetic flux generated by the coil can minimized ,and so eddy current within the first and second internal conductors can be prevented from generating.

[0018] Further, the chip is shaped like a rectangular solid and the insulating material sheets are shaped like a square, and further the first lead internal conductor is exposed to the four surfaces of the chip which are parallel to the winding center-line of the coil. Therefore, even when the external terminal electrode is formed on any face of the four surfaces, the same multi-laminated inductor may be obtained. Further, by forming a second lead internal conductor at varied position in the production of the coil, the position of connection between the second lead internal conductor and an end portion of the coil can be changed. Thus, the value of inductance can be easily changed.

[0019] Also, according to the invention, the multi-laminated inductor described above is provided with a rectangular solid-shaped chip having square-shaped sheets of insulating material laminated and further provided with a lead layer made of an insulating material sheet having a first lead internal conductor formed thereon and an insulating sheet having a second lead internal conductor formed thereon, wherein the first lead internal conductor is formed along a diagonal of the insulating material sheet and both ends thereof each are formed like a linear shape with a predetermined width extending over two sides, the second lead internal conductor being formed like a linear shape with a predetermined width and being placed so that one end thereof may be connected to the first lead internal conductor nearly at the center of the insulating material sheet and the other end thereof may be connected to a predetermined spot of the end of the coil.

[0020] This multi-laminated inductor has the first and second lead internal conductors establishing an electrical connection between an end of the coil and an external terminal electrode. Since these first and second lead internal conductors are formed like a linear shape, the area intersecting the magnetic flux generated by the coil can be minimized. Thus, Eddy current can be prevented from generating within the first and second lead internal conductor. Also, the chip is shaped like a rectangular solid and the insulating material sheets are shaped like a square, and the first lead internal conductor is exposed to the four chip surfaces parallel to the winding center-line of the coil. Therefore, even when the external terminal electrode is formed on any one of the four surfaces, the same multi-laminated inductor can be obtained. Further, by forming the second lead internal conductor at a varied position in the manufacturing, the second lead internal conductor can be connected to the varied end of the coil. Thus, the value of inductance can be easily varied.

[0021] Also, according to the invention, in the multi-laminated inductor described above, the external terminal electrodes are disposed at both end portions along the winding center-line and portions thereof are continuously spread over the peripheries of the adjoining faces.

[0022] As this multi-laminated inductor can provide a long distance between two external terminal electrodes, when mounted on a board it can reduce the stress produced at the external terminal electrodes due to the bending of the board. Thus, the occurrence of connection failure between the electrodes on the board and the external terminal electrodes can be reduced.

[0023] Further, according to the invention, the multi-laminated inductor described above is provided with the external terminal electrodes formed on both end portions, along the winding center-line of a coil, in each of the two faces nearly parallel to the winding center-line of the coil and adjacent to the face which are opposed to a board surface when mounted on the board and parallel to an orbital centerline of the coil.

[0024] This multi-laminated inductor can provide a long distance between the external terminal electrodes which are formed on both end portions along the winding center-line of the coil. Therefore, when the inductor is mounted on a board, the stress produced at the exter-

nal terminal electrodes due to the bending of the board can be reduced. Further, the multi-laminated inductor allows to be mounted on a board so that the external terminal electrodes may be perpendicular to the board surface. Pairs of the external terminal electrodes are disposed, respectively, on the two surfaces of the chip that are perpendicular to the board surface. Thus, at the time of reflow, the Manhattan phenomenon that a chip rises up can be prevented from occurring.

[0025] Also, according to the invention, the multi-laminated inductor is made of a coil having a winding layer having a coil conductor formed and a lead layer laminated outside the turn layer, and of external terminal electrodes formed on a chip surface nearly parallel to the winding center-line of the coil and connected to the lead internal conductors. When the multi-laminated inductor described above is manufactured, by changing the position where the lead internal conductor is disposed on the insulating material sheet making up the lead layer, the position where the lead internal conductor is connected to the coil end can be changed. Thus, the multi-laminated inductor of different inductance values can be obtained.

[0026] Further, in this manufacturing method, internal conductors shaped like a letter I, L or U and via holes to be connected to the end portion thereof are formed on insulating material sheets. Then, the winding layer is formed by laminating a plurality of these insulating material sheets so that the internal conductors may form a coil. Also, the lead layer comprises one or more insulating material sheets on each of which a lead internal conductor having one end thereof connected to a coil end and the other end thereof reaching to an edge of the sheet is formed.

[0027] According to this manufacturing method of the multi-laminated inductor, by changing the position where the lead internal conductor is connected to a coil end, there is made a portion of the coil end which does not function as a coil. Thus, inductance values can be changed.

[0028] Further, in the manufacturing method described above, only changing the position to form the lead internal conductor allows a change or adjustment of the value of inductance. Therefore, at the time of manufacturing, only the preparation of insulating material sheets having the lead internal conductor formed at a varied position allows easy manufacturing of the multi-laminated chip inductors with a different value of inductance, without changing the outside shape and the position of the external terminal electrodes.

[0029] Therefore, the adjustment of an inductance value does not require extensive redesigns such as changing the core area as previously needed. Further, it is not necessary extensively to change the content of design for each different value of inductance. Thus, it is very simple to control the design specification.

[0030] Also, in the manufacturing method for the multi-laminated inductor described above, an internal conductor making up a coil end and at least a portion of a lead internal conductor are opposed and connected to each other without existence of the insulating material sheet between them. For this, an insulating material sheet having a lead internal conductor or an internal conductor making up the coil end formed thereon is laminated on the other insulating material sheet with reverse from top to bottom so that the structure described just above may be obtained.

[0031] According to this manufacturing method, when the inductance value is varied by changing the position to form the lead internal conductor, even in cases where two or more insulating material sheets require some modification such as through-hole machining, this variation is possible only by changing one insulating material sheet having the lead internal conductor formed. That is, an insulating material sheet having a lead internal conductor or an internal conductor making up the coil end formed thereon is laminated on the other insulating material sheet with reverse from top to bottom.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

FIG. 1 is a perspective diagram showing a multi-laminated chip inductor of a first embodiment of the invention;

FIG. 2 is a perspective diagram showing a typical example of a conventional multi-laminated chip inductor;

FIG. 3 is a perspective diagram showing a longitudinal stack type of a multi-laminated chip inductor;

FIG. 4 is a representation of a laminated structure of a example of a conventional longitudinal staked type of a multi-laminated chip inductor;

FIG. 5 is a diagram illustrating problems of conventional types;

FIG. 6 is a diagram showing a laminated structure of a multi-laminated chip inductor of the first embodiment of the invention;

FIG. 7 is a diagram showing the relation between external terminal electrodes of the first embodiment of the present invention and the magnetic flux;

FIG. 8a to 8g are illustrations of the relation between the positions of lead internal conductors of the first embodiment of the invention and the inductance values;

FIG. 9 is a diagram showing the lead internal conductors of the first embodiment of the invention chip surfaces;

FIG. 10 is a diagram showing other shapes of the lead internal conductors of the first embodiment of the invention;

FIG. 11 is a diagram showing other exposure situation where the chip surface, of the lead internal conductors of the first embodiment of the present invention is exposed to chip surfaces;

FIG. 12 is a diagram showing a laminated structure of a second embodiment of the invention;

FIG. 13a to 13g are illustrations of the relation between the positions of lead internal conductors of the second embodiment of the invention and inductance values;

FIG. 14 is a diagram showing a laminated structure of a multi-laminated chip inductor according to a third embodiment of the present invention;

FIG. 15 is a diagram showing a different example of external terminal electrode formation of an embodiment of the invention;

FIG. 16 is a diagram showing a different example of external terminal electrode formation of an embodiment of the invention;

FIG. 17 is a diagram showing a different example of external terminal electrode formation of an embodiment of the invention;

FIG. 18 is an illustration of the exposure position of an end of the lead internal conductor related to a different example of the external terminal electrode formation of an embodiment of the present invention;

FIG. 19 is an illustration of the exposure position of an end of the lead internal conductor related to a different example of the external terminal electrode formation of an embodiment of the present invention;

FIG. 20 is an illustration of the exposure position of an end of the lead internal conductor related to a different example of the external terminal electrode formation of an embodiment of the present invention;

FIG. 21 is an illustration of inductance when the multi-laminated chip inductor of an embodiment of the invention is mounted on a parent circuit board;

FIG. 22 is an illustration of inductance when the multi-laminated chip inductor of an embodiment of the invention is mounted on a parent circuit board;

FIG. 23 is an illustration of inductance when the multi-laminated chip inductor of an embodiment of the invention is mounted on a parent circuit board;

FIG. 24 is an illustration of a different formation position of the external terminal electrode and the exposure position of an end of the lead internal conductor according to an embodiment of the invention;

FIG. 25 is an illustration of inductance when the multi-laminated chip inductor of an embodiment of the invention is mounted on a parent circuit board;

FIG. 26 is a diagram showing a different example of the lead internal conductor formation according to an embodiment of the invention;

FIG. 27 is a diagram showing a different example of the lead internal conductor formation according to an embodiment of the invention;

FIG. 28 is a diagram showing a different example of the lead internal conductor formation according to an embodiment of the invention; and

FIG. 29 is a diagram showing a different example of the lead internal conductor formation according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0033] The details of the present invention will be explained with reference to the appended drawings.

[0034] FIG. 1 is a schematic perspective diagram of a multi-laminated chip inductor 10 according to a first embodiment of the invention and FIG. 6 is an illustration of a laminated structure thereof. Referring to FIG. 1, a chip 11 has the geometry of a rectangular solid with a laminated structure made of an electrically insulating magnetic or non-magnetic material. A coil 12 is formed to be internal conductors which are buried in the chip 11, and connected in a helical shape. Also, external terminal electrodes 13a, 13b are formed on the same chip surface parallel to the center line 12a of windings of the coil 12.

[0035] Here, the coil 12 is formed so that its winding center-line 12 may extend along the direction of laminating in the laminated structure of the chip 11.

[0036] The chip 11, as shown in FIG. 6, is formed by laminating two or more sheets 21 to 26 of insulating material with a predetermined thickness having the geometry of a square.

[0037] In the following explanation, the insulating material sheets 21 to 26 are assumed to be laminated along the up-and-down direction corresponding to FIG. 6.

[0038] That is, the chip 11 comprises a winding layer 11a, lead layers 11b and 11c, and dummy layers 11d and 11e.

[0039] The winding layer 11a is a layer for forming the coil 12. This winding layer 11a is formed by laminating a plurality of square insulating material sheets 21, which have on its top an internal conductor 21a shaped like a letter U having a via hole 21b at one end thereof filled with a conductor. When these insulating material sheets 21 are laminated, one end of the internal conductor 21a on an upper layer is connected to the other end of the conductor 21a on the adjoining lower layer through a conductor in the via hole. Thus, the internal conductors 21a formed on two or more layers makes the helical coil 12.

[0040] In the explanation below, a via hole filled with a conductor will be referred to simply as a via hole. It is assumed that "connected to a via hole" and "connected by a via hole" mean "connect to the conductor filled in a via" and "connected by the conductor filled in a via," respectively.

[0041] The lead layer 11b is placed on the winding layer 11a. This lead layer 11b comprises an insulating material sheet 22 having a lead internal conductor 22a formed on its top and an insulating material sheet 23 having a lead internal conductor 23a formed on its top.

[0042] One lead internal conductor 22a has one end thereof positioned in the middle of the sheet 22 and the other end thereof disposed to connect to a via hole 22b formed at a predetermined position. The via hole 22b is connected to the other end of the internal conductor 21a on the highest layer of the winding layer 11a.

[0043] Further, the other lead internal conductor 23a is formed like a cross with a minimal width necessary for connecting to a via hole 23b formed in the middle of the sheet 23. The four ends of the conductor 23a reach to nearly the middle of the four sides of the sheet 23, respectively. Also, the via hole 23b is connected to the one end 22c of the lead internal conductor 22a described above.

[0044] Thereby, the lead internal conductor 23a is exposed to the four surfaces of the chip 11, respectively, having a linear shape with a predetermined length.

[0045] The lead layer 11c, placed under the winding layer 11a, comprises an insulating material sheet 24 having a lead internal conductor 24a formed on its top and an insulating material sheet 25 having a lead internal conductor 25a formed on its top.

[0046] Also, one lead internal conductor 24a is formed so that one end thereof may be connected to a via hole 24b formed in the middle of the sheet 24 and the other end thereof may be connected to a via hole 21b in the bottom layer of the winding layer 11a.

[0047] Further, the other lead internal conductor 25a is shaped like a cross which has its intersection in the middle of the sheet 25 and a minimal width necessary for connecting to the via hole 24b formed in the sheet 24. The four ends of the conductor 25a reach to the middle of the four sides of the sheet 25, respectively.

[0048] Thereby, the lead internal conductor 25a is exposed to the four surfaces of the chip 11, having a linear shape with a predetermined length.

[0049] Each of the dummy layers 11d and 11e is made of two or more insulating material sheets 26 that have no internal conductor formed. One dummy layer 11d is disposed on the lead layer 11b and the other dummy layer 11e is disposed under the lead layer 11c.

[0050] The multi-laminated chip inductor 10 described above does not have external terminal electrodes formed on both end faces along the chip length which are perpendicular to the winding center-line 12a of the coil 12. Therefore, a magnetic flux ϕ generated by the passage of electric current through the coil does not intersect the external terminal electrodes 13a and 13b. Thus, eddy current within the external terminal electrodes 13a and 13b can be prevented generating, so that electrical loss can be made less than conventional types.

[0051] Also, in the structure described above, the magnetic flux generated by the coil 12 intersects the lead internal conductors 22a, 23a, 24a and 25a. However, the areas of these lead internal conductors can be decreased to minimal areas required for conduction of electricity, so that the generation of eddy current is made extensively less than in previous types and the production of losses can be suppressed.

[0052] Further, the internal conductors 21a forming the coil 12 and the external terminal electrodes 13a and 13b are disposed so that their respective planes may be perpendicular to each other. Therefore, the stray capacity between them is extensively reduced when compared to conventional types, so that a decrease in self-resonance frequency can be suppressed.

[0053] Also, in the multi-laminated chip inductor 10a of the structure described above, the inductance values corresponding to 0 through 3/4 turn can be easily varied by changing the connection position between the lead internal conductor layer 22a and the internal conductor 21a of the highest layer in the winding layer 11a.

[0054] For example, when the via hole 22b formed at the other end of the lead internal conductor 22a is matched to the other end 21c of the internal conductor 21a on the highest layer of the winding layer 11a, as shown in FIG. 8a, a maximum inductance in the structure described above can be obtained.

[0055] Also, various inductance values can be obtained by positioning the via hole 22b formed at the other end of the internal conductor 22a to the various positions as shown in FIG. 8b to 8g. The structure as shown in FIG. 8b reduces inductance by a inductance value corresponding to 1/8 turn. Also, The structures of FIGS. 8c, 8d, 8e, 8f and 8g provide decreases corresponding to 1/4 turn, 3/8 turn, 1/2 turn, 5/8 turn and 3/4 turn, respectively.

[0056] Thus, only by preparing various insulating material sheets 22 with the lead internal conductor 22a formed at different positions at the time of manufacturing, different values of inductance can be manufactured without the need for changing the outside shape and the formation position of the external terminal electrodes 13a and 13b.

[0057] Thus, concerning the production of the multi-laminated chip inductor described above, adjusting the value of inductance does not require extensive redesigns such as changing core areas, though needed for conventional types, and further extensively changing the content of design is not necessary for each different value of inductance. Therefore, it is very simple to control design specification and so on.

[0058] Further, it is also possible to change the value of inductance in the same way by changing both the formation position of the lead internal conductor 24a and the formation position of the via hole 21b in the insulating material sheet 21 of the lowest layer in the winding layer 11a. However, in this case, it is necessary to vary two insulating material sheets.

[0059] Next, the method for manufacturing the multi-laminated chip inductor described above will be explained.

[0060] First, green-sheets are made of slurry composed of low-temperature burning insulating materials by using the doctor blade method.

[0061] Further, the via holes described above are formed at the necessary positions of the green-sheets. Then, a conductor paste including silver as a major constituent is printed on the green-sheets described above with a predetermined pattern by using screen-printing so that the via holes described above may be filled with the paste. After that, the printed green-sheets are laminated so that conductor pastes can be bonded to each other through the via holes for forming the coil 12.

[0062] Still, at the time of manufacturing, internal conductors corresponding to two or more multi-laminated chip inductors are formed on one green-sheet, and two or more green-sheets having internal conductors formed are laminated in the same way. Thus, two or more multi-laminated chip inductors are made at the same time.

[0063] Next, the laminated assembly described above is made into a single body by thermocompression bonding.

[0064] After the body is cut and separated into each individual multi-laminated chip inductor, the chip inductors are heated in the atmosphere to remove binder from the green-sheets (binder removing treatment) and then are burned at 900°C for 1hr in the atmosphere.

[0065] As shown in FIG. 9, the burned product (chip 11) obtained by this process has the ends of the lead internal conductors 23a and 25a exposed respectively in the four chip surfaces almost parallel to the winding center-line 12a of the coil 12.

[0066] An electrode paste including glass-frit having silver as a major constituent are printed on the burned product by using screen printing and baked, so that the external terminal electrodes 13a and 13b electrically connected to the exposed portions of the lead internal conductors 23a and 25a are formed.

[0067] Further, the external terminal electrodes 13a and 13b are plated with nickel and solder. Thus, the multi-laminated chip inductor is completed.

[0068] Here, the lead internal conductors 23a and 25a are exposed to the four surfaces of the chip 11, respectively. Therefore, when a pair of the external terminal electrodes 13a and 13b described above is formed in the same surface of the chip 11, it is not necessary to select a direction of the chip 11. Thus, the productivity can be improved.

[0069] The shape of the lead internal conductor exposed to the surfaces of the chip 11 is not limited to a cross-like shape described above. For example, as a substitute for the cross-shape lead internal conductor, use of lead internal conductors 23a' and 25a' as shown in FIG. 10 can achieve the same effect.

[0070] That is, lead internal conductors 23a' and 25a' with a predetermined width are formed along a diagonal line on the top of the sheets 23 and 25. Thereby, each of the lead internal conductors 23a' and 25a' has both ends which are spread over both of two adjoining sides and exposed to the four surfaces of the chip 11, respectively, in the shape of a linear geometry with a predetermined length.

[0071] Therefore, at the time of manufacturing, for forming external terminal electrodes 13a and 13b, it is not necessary to select a direction of the chip. Thus, productivity can be improved.

[0072] Next, a second embodiment of the invention will be explained.

[0073] FIG. 12 is an illustration of a multi-laminated structure of a multi-laminated chip inductor according to a second embodiment, and it has the same appearance as the first embodiment as shown in FIG. 1.

[0074] Referring now to FIG. 12, the same components as the first embodiment described above are shown by the same reference sign and so their explanation will be omitted. Also, the difference between the first embodiment and the second embodiment is as follows. That is, an internal conductor 21a' of the lowest layer in the winding layer 11a may be formed on the bottom surface of the insulating material sheet 21. With laminating this sheet 21 with downward internal conductor 21a', the inductance value can be easily changed in the range of inductance corresponding to 0 through 3/4 turn by changing the placement of the lead internal conductor 24a.

[0075] That is, as shown in FIG. 12, the internal conductor 21a' of the lowest layer in the winding layer 11a is formed like a letter U on the bottom surface of the insulating material sheet 21. Here, a via hole 21b formed at one end of the internal conductor 21a' is formed so as to connect to a via hole 21b formed in the next higher insulating material sheet 21. Further, it is needless to say that the internal conductor 21a' is disposed to connect with other internal conductor 21a of the winding layer 11a for forming the coil 12.

[0076] Further, the lead internal conductor 24a of the lead layer 11c has the other end connected to a predetermined spot of the internal conductor 21a'.

[0077] According to the structure described above, when the position of the other end of the lead internal conductor 24a is matched to the other end 21c' of the internal conductor 21a' of the lowest layer in the winding layer 11a as shown in FIG. 13, the decrease of inductance caused by the formation position of the lead internal conductor 24a is 0 when compared to the first embodiment.

[0078] Also, by forming the lead internal conductors 24a so that the other end of the conductors 24a may be disposed at the positions as shown in FIGS. 13b to 13g, various values of inductance can be obtained as follows. For the structure of FIG. 13b, an inductance value corresponding to 1/8 turn is reduced. For the structures of FIGS. 13c, 13d, 13e, 13f and 13g, inductance values corresponding to 1/4 turn, 3/8 turn, 1/2 turn, 5/8 turn and 3/4 turn are reduced, respectively.

[0079] Thereby, at the time of manufacturing, only by preparing insulating material sheets 24 with the lead internal conductors 24a formed at different positions, it is possible to manufacture multi-laminated chip induc-

tors with various value of inductance. Also, without changing the outside shape and the formation position of the external terminal electrodes 13a and 13b, the inductance values in the range corresponding to 0 through 3/2 turn can be easily varied in accordance with the variable amount of inductance corresponding to the formation position of the lead internal conductor 22a.

[0080] Thus, concerning the manufacturing of the multi-laminated chip inductor described above, extensive re-designs such as changing the core area, needed by conventional types, is not required for adjusting the value of inductance, and further it is not necessary to extensively change design for each of different values of inductance. It is very simple to control design specification.

[0081] Further, it is needless to say that the second embodiment can obtains the same effect as the first embodiment.

[0082] Next, the third embodiment of the invention will be explained.

[0083] FIG. 14 is an illustration of a laminated structure of a multi-laminated chip inductor according to a third embodiment, and it has the same appearance as the first embodiment.

[0084] Also, in FIG. 14, the same components as the second embodiment described above are shown by the same reference signs, and the explanation of them will be omitted.

[0085] Further, the difference between the second and third embodiments is in the changed structure of the lead layers 11b and 11c.

[0086] That is, the lead layer 11b is made of an insulating material sheet 27 shaped like a square with a predetermined thickness which has a lead internal conductor 27a with a predetermined width in the shape of a linear geometry disposed on the bottom surface thereof. This lead internal conductor 27a is formed so as to have one end reaching to an edge of the insulating material sheet 27 and a minimum length required for the other end to be connected to a predetermined position of the opposite internal conductor 21a.

[0087] Also, the lead layer 11c is made of an insulating material sheet 28 shaped like a square with a predetermined thickness. Further, the sheet 28 has a lead internal conductor 28a with a predetermined thickness in the shape of a linear geometry disposed on the top surface thereof. This lead internal conductor 28a is shaped to a minimum length so that one end thereof may reach to the edge of the insulating material sheet 28 at the same side as the one end of the lead internal conductor 27a, and the other end thereof may be connected to a predetermined spot of the opposite internal conductor 21a'.

[0088] According to the multi-laminated chip inductor described above, the external terminal electrodes 13a and 13b are not formed on both faces along the chip length perpendicular to the winding center-line 12a of the coil 12. Therefore, the magnetic flux ϕ generated by the passage of electric current through the coil does not intersect the external terminal electrodes 13a and 13b, so that electrical loss can be made less than conventional types.

[0089] Further, the internal conductors 21a forming the coil and the external terminal electrodes 13a and 13b are disposed so that their respective planes may be perpendicular to each other. Therefore, the stray capacity between them is extensively reduced when compared to conventional types, so that a decrease in self-resonance frequency can be suppressed.

[0090] Still further, in the structure described above, since the lead internal conductors 27a and 28b are formed on the periphery of the insulating material sheets 27 and 28, the magnetic flux generated by the coil does not almost intersect with the lead internal conductors 27a and 28a. Thus, the generation of eddy current can be reduced when compared to the first and second embodiments, and so electrical loss can be suppressed.

[0091] Also, by changing the connection position between the lead internal conductor 27a and the internal conductor 21a of the highest layer in the winding layer 11a, or the connection position between the lead internal conductor 28a and the internal conductor 21a of the lowest layer in the winding layer 11a, it is easy to change the inductance value in the range corresponding to 0 through 1/2 turn.

[0092] Thereby, only by preparing various insulating material sheets 27 and 28 having the lead internal conductor 27a and 28a formed at different positions at the time of production, different values of inductance can be easily produced without the need for changing the outside shape and the formation position of the external terminal electrodes 13a and 13b.

[0093] Thus, in the production of the multi-laminated chip inductor described above, adjusting the value of inductance does not require extensive re-designs such as changing core areas, needed by conventional types, and further extensive change of the design content is not necessary for each different value of inductance. Therefore, it is very simple to control design specification and so on.

[0094] Still, the multi-laminated chip inductor of the second embodiment is not limited to the structure described above. For example, the multi-laminated chip inductors having the external terminal electrodes formed at the position as shown in FIGS. 15 through 17 can achieve the same effect described above.

[0095] The external terminal electrodes 14a and 14b of the multi-laminated chip inductor 10 as shown in FIG. 15 are connected to the lead internal conductors which are exposed to the same surface parallel to the winding center-line 12a of the coil 12. Further, the external terminal electrodes 14a and 14b are disposed on the both end portions along the length of this face and portions thereof covers continuously the peripheries of other three adjoining surfaces. Even this structure also can provide a long distance between the two external termi-

nal electrodes 14a and 14b. Thus, when mounted on a board, this structure can reduce the stress produced between the external terminal electrodes 14a and 14b due to the bending of the board, so that the occurrence of poor connections can be reduced.

[0096] Also, the external terminal electrodes 15a and 15b of the multi-laminated chip inductor 10 as shown in FIG. 16 are connected to the lead internal conductors which are exposed to the same surface parallel to the winding center-line 12a of the coil 12. Further, the external terminal electrodes 15a and 15b are disposed on the both end portions along the length of this surface and portions thereof covers continuously the peripheries of the end faces along the length of the chip 11. Even this structure also can provide a long distance between the two external terminal electrodes 15a and 15b. Thus, when this structure is mounted on a board, the occurrence of poor connections due to the bending of the board can be reduced.

[0097] Also, the external terminal electrodes 16a and 16b of the multi-laminated chip inductor 10 as shown in FIG. 17 are connected to a lead internal conductor of one end side of the coil 12, and the external terminal electrodes 17a and 17b are connected to a lead internal conductor of the other end side of the coil 12. Further, these electrodes 16a, 16b, 17a and 17b are disposed in each of the two surfaces adjacent to the chip face facing the board on which the multi-laminated chip inductor 10 is mounted. That is, the external terminal electrodes 16a and 17a are disposed at both end portions along the chip length in the same surface, respectively, and the electrodes 16b and 17b are disposed on both end portions along the length in the surface opposed to this surface.

[0098] Even this structure also can provide a long distance between the external terminal electrodes on both end portions along the length of the chip. Thus, when this structure is mounted on a board, the occurrence of poor connections due to the bending of the board can be reduced. Further, a pair of the external terminal electrodes is so formed as to be perpendicular to the board on each of the both end portions along the length of the chip 11. Therefore, at the time of reflowing, the rising of the chip, namely Manhattan phenomenon, can be prevented.

[0099] Further, as shown in FIG. 17, the external terminal electrodes 16a, 16b, 17a and 17b are formed on each of the two faces adjacent to the chip face opposed to the parent board surface on which the chip is mounted. In this case, the placement of the lead internal conductors to be described below provides the nearly same value of inductance, even if the chip is mounted with a reverse direction from top to bottom.

[0100] For example, as shown in FIG. 18, two lead conductors 41 and 42 are disposed so that a distance between a position having one lead conductor 41 exposed (the connection position of the external terminal electrodes 16a and 17a) and the top face of the chip may be made equal to the distance between the position having the other lead conductor 42 exposed (the connection position of the external terminal electrodes 16b and 17b) and the bottom surface of the chip.

[0101] By this placement of the lead conductors 41 and 42, the sum of the respective distances between the lead conductors 41 and 42 and the lands 31 and 32 becomes always a constant value ($D0 = D1 + D2$), even if either of the top and bottom faces of the chip 11 of FIG. 8 is opposed to the parent circuit board 30, as shown in FIG. 19 and 20.

[0102] In general, as shown in FIGS. 21 through 23, when the inductor 10 is mounted on a parent circuit board 30, the external terminal conductors 16a, 16b, 17a and 17b are soldered to lands 31 and 32. Then, inductances Lx1 through Lx4 are produced along the external terminal electrodes 16a, 16b, 17a and 17b due to the solder portions, respectively. These inductance values depend on the distances between the lands 31 and 32 and the exposed ends of the lead conductors 41 and 42. Therefore, as described above, the lead conductors 41 and 42 are disposed so that the sum of the respective distances from the exposed ends of the lead conductors 41 and 42 to the lands 31 and 32 can be always a constant value ($D0 = D1 + D2$). Thus, the sum of the inductances Lx1 through Lx4 is always a constant value. That is, the sum of the inductances Lx1 through Lx4 when the multi-laminated chip inductor 10 is mounted on the parent circuit board 30 as shown in FIG. 22 is equal to the sum of the inductance Lx1' through Lx4' when mounted with the reverse from top to bottom as shown in FIG. 23.

[0103] Also, as shown in FIG. 24, both end faces along the length of the chip 11 are shaped like a square and individual external terminal electrodes 51a through 51d are formed respectively on four side faces except these both end faces. Even when the external terminal electrodes 51b, 51d, 52b and 52d nearly perpendicular to the board face of a parent circuit board 30 are soldered to the lands 31 and 32, the lead internal conductors 53 and 54 are formed in the same described above. So, even if the multi-laminated chip inductor 10 is mounted with the reverse from top to bottom, the inductance value has only a slight variation.

[0104] That is, as shown in FIG. 25, the sum of the inductances Lx1 through Lx4 produced by soldering varies little whichever face of the chip 11 is downward when the multi-laminated chip inductor is mounted on the parent board 11.

[0105] Further, in the multi-laminated chip inductor of the first embodiment described above, as shown in FIG. 26, the lead internal conductors 22a and 24a shaped like a linear geometry and the lead internal conductors 23a and 25a shaped like a cross may be connected through via holes 61 made of a plurality of via holes connected in series. Such structure can increase the distance between the coil 12 and the lead internal conductors 23a and 25a shaped like a cross, and allows

the external terminal electrodes 13a and 13b to be separated from the coil 12. Therefore, the stray capacity produced between the coil 12 and the external terminal electrodes 13a and 13b can be reduced.

[0106] Also, as shown in FIG. 27, an internal conductor 62a forming an end of the coil 12 is extended to an edge of an insulating material sheet 62. The edge portion 62a of the extended internal conductor is exposed to the surface of the chip 11 for use as a lead internal conductor 63. By this structure, it is also possible to form external terminal electrodes on a chip surface parallel to the winding center-line 12a of the coil 12. Thus, Eddy current generated in the external terminal electrodes can be reduced.

[0107] Further, as shown in FIG. 28, the lead internal conductors 64a and 64b is made thicker at their portions close to the surface. This increases the area of the conductors 64a and 64b exposed to the surface of the chip 11 and so improves connectivity with the external terminal electrodes 65a and 65b. In this case, to increase the thickness of the lead internal conductors 64a and 64b, two or more times coating of electrically conductive paste may be used when these conductors 64a and 64b are formed at the time of production.

[0108] Also, as shown in FIG. 29, lead internal conductors 67a and 67b are formed on the opposite face of the insulating material sheets 26 and 21 adjacent to the insulating material sheet 64 having the lead internal conductor 64a and 64b. And, the faces of these internal conductors are opposite to each other and connected to provide thicker conductors. These and other methods can be used to easily increase the thickness of the lead internal conductors.

[0109] Also, as a low-temperature burned insulating material used for the manufacturing of the multi-laminated chip inductor described above, magnetic materials such as Ni-Zn based ferrite et al. may be used. Further, as an internal conductor, other metals such as silver-palladium alloy, silver-platinum alloy, gold et al. may be used. In addition, metals other than silver may be used for the external terminal electrodes.

[0110] Also, the reverse-coater and others may be used for forming green sheets, and the slurry build method and others may be used as a method for laminating. The internal conductors may be formed by other methods such as transcription and sputtering.

[0111] Further, the external terminal electrodes may be formed by sputtering and other methods, and other metals may be used for plating them.

[0112] The descriptions described above of the conventional technology, means for solving problem, and description of the preferred embodiment are necessary and sufficient for explaining the content of the invention to persons skilled in the art.

[0113] Further, it is needless to say that the invention is not limited to the structures of the embodiments described above.

Claims

1. A multi-laminated inductor comprises a chip with a laminated structure having a coil buried therein and an external terminal electrode formed on a surface of said chip and connected to an end of said coil, comprising:

   a lead layer having a lead internal conductor that is being exposed to a chip surface nearly parallel to a line passing through the winding central portion of said coil and connected to an end of said coil; and
   an external terminal electrode formed on a face nearly parallel to said line passing through the winding central portion of said coil and connected to said lead internal conductor.

2. The multi-laminated inductor according to claim 1, wherein said lead internal conductor is exposed to all faces nearly parallel to said line passing through the winding central portion of said coil.

3. The multi-laminated inductor according to claim 1, wherein said chip has the geometry of a rectangular solid having square-shaped sheets of insulating material laminated, said lead layer comprising an insulating material sheet having a first lead internal conductor formed and an insulating sheet having a second lead internal conductor formed,

   said first lead internal conductor having the shape of a cross with a predetermined width, its intersection point at the center of said insulting material sheet and its four ends reaching to the edges of said insulating material sheet, and said second lead internal conductor having a linear shape with a predetermined width and having one end thereof connected to said first lead internal conductor nearly at the center of said insulating material sheet and the other end thereof formed at a position connecting to a predetermined spot of said end of said coil.

4. The multi-laminated inductor according to claim 1, wherein said chip has the geometry of a rectangular solid having square-shaped sheets of insulating material laminated, said lead layer comprising an insulating material sheet having a first lead internal conductor formed and an insulating sheet having a second lead internal conductor formed,

   said first lead internal conductor being formed on a diagonal of said insulting material sheet and having each of both ends thereof extended over two sides with a linear shape having a predetermined width, and
   said second lead internal conductor having a

linear shape with a predetermined width and having one end thereof connected to said first lead internal conductor nearly at the center of said insulating material sheet and the other end thereof formed at a position connecting to a predetermined spot of said end portion of said coil.

5. The multi-laminated inductor according to claim 1, wherein said external terminal electrodes are formed on both end portions along the direction of said line passing through the winding central portion of said coil and portions thereof are continuously spread on peripheries of adjoining faces.

6. The multi-laminated inductor according to claim 1, wherein said external terminal electrodes are formed on each of both end portions along said line passing through the winding central portion of said coil in two faces parallel to said line passing through the winding central of said coil and the two faces having said external terminal conductor formed are adjacent to the face which is opposed to a board surface when the multi-laminated inductor is mounted on the board and parallel to said line passing through the winding central portion of said coil.

7. A method of manufacturing a multi-laminated inductor comprising a winding layer which is made by laminating a plurality of insulating material sheets having internal conductors formed on the surface like a letter I, L or U and having a via hole connected to an end portion of said internal conductor formed so that said internal conductors may form a coil, and a chip comprising one or more insulating material sheet on which a lead internal conductor having one end thereof connected to an end portion of said coil and the other end thereof reaching to an edge of a sheet is formed and having a lead layer laminated outside said winding layer, and an external terminal electrode formed on a chip surface nearly parallel to said line passing through the winding central portion of said coil and connected to said lead internal conductor, which includes;

manufacturing a multi-laminated inductor of different inductance value by changing the position where the lead internal conductor is formed on an insulating material sheet making up said lead layer so as to change a position to connect said lead internal conductor to said end portion of said coil.

8. The method of manufacturing a multi-laminated inductor according to claim 7, wherein an insulating material sheet having a lead internal conductor or a internal conductor making up a coil end formed thereon is laminated on the other insulating material sheet with reverse from top to bottom so that the internal conductor making up the end of said coil and at least a portion of said lead internal conductor may be opposed and connected to each other without any an insulating material sheet between them.

Fig. 1

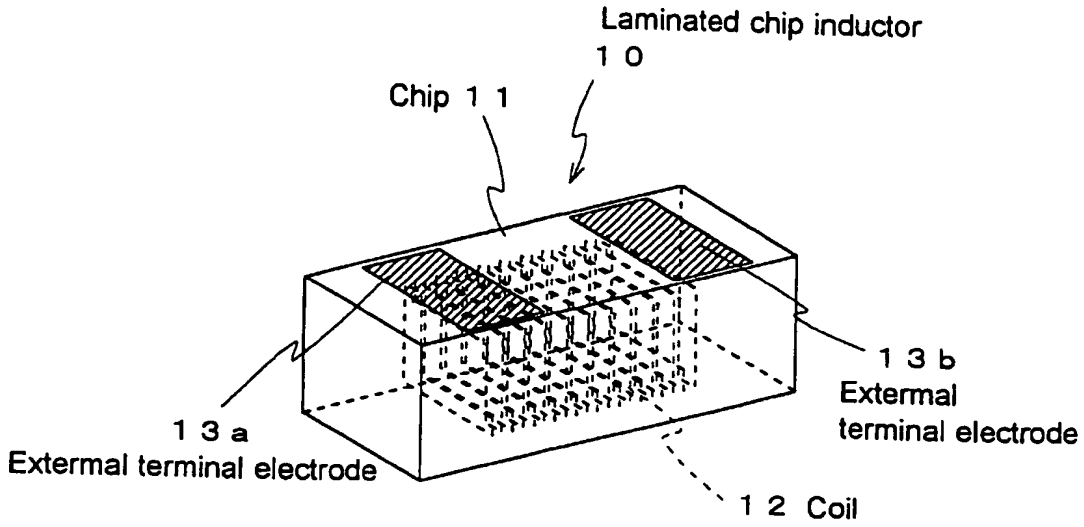

Laminated chip inductor
1 0
Chip 1 1
1 3 b
External
terminal electrode
1 3 a
External terminal electrode
1 2 Coil

Fig. 2

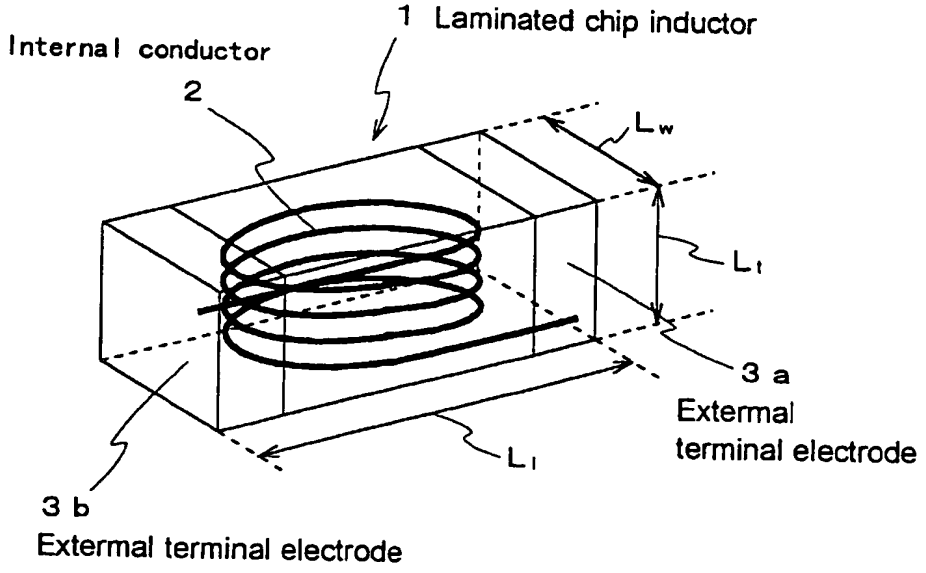

1 Laminated chip inductor
Internal conductor
2
Lw
Lt
3 a
External
terminal electrode
Ll
3 b
External terminal electrode

Fig. 3

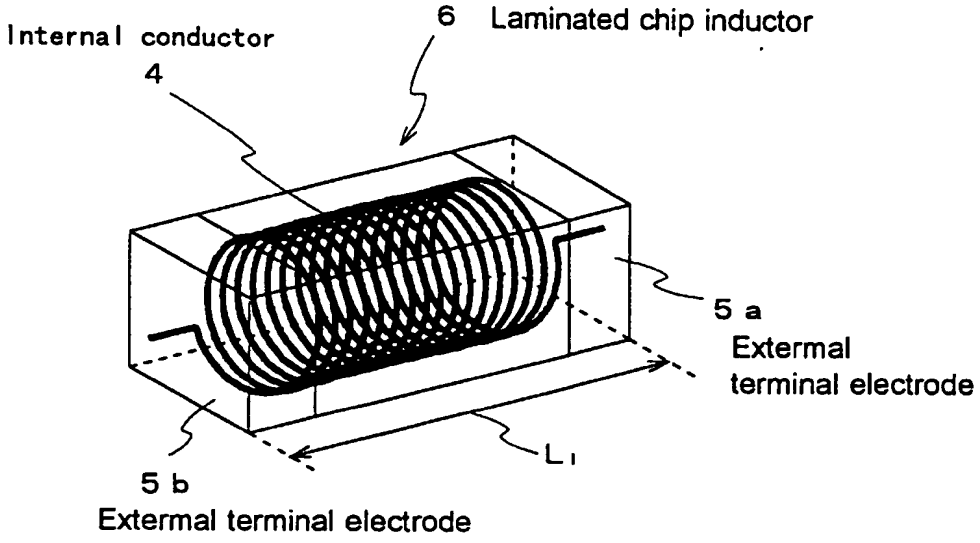
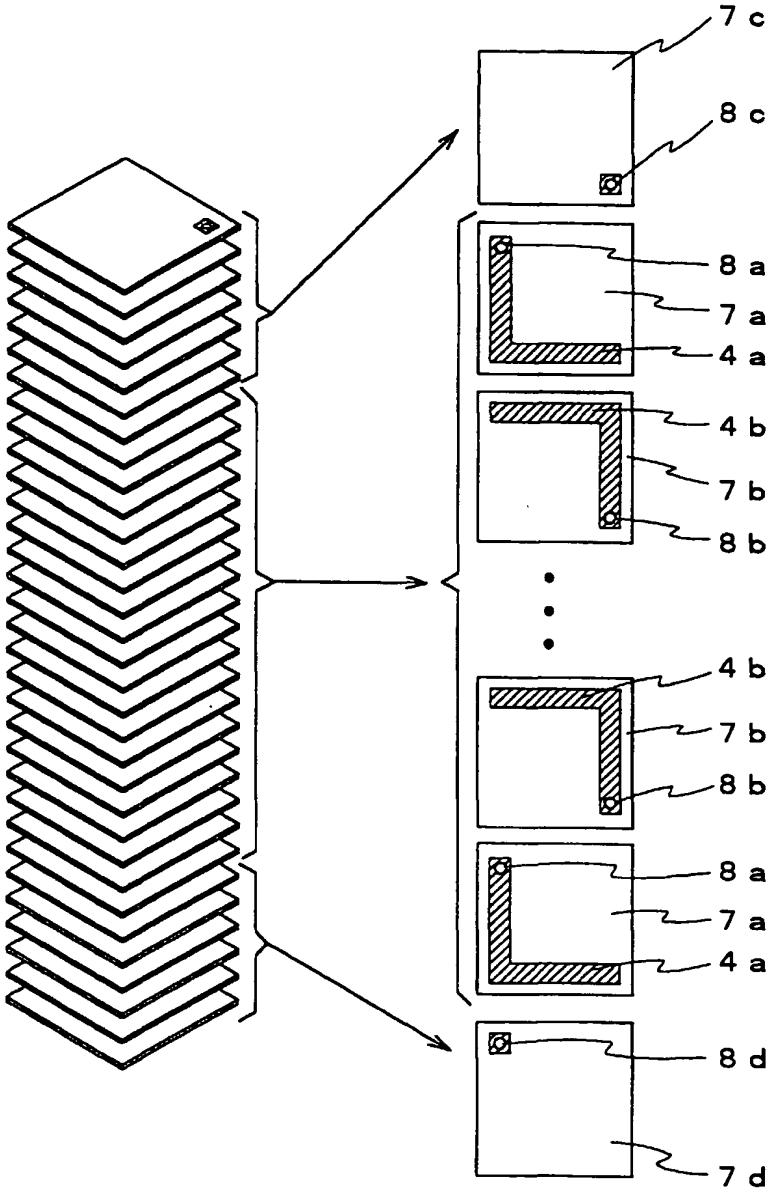

Internal conductor
4
6 Laminated chip inductor
5 a
External
terminal electrode
5 b
External terminal electrode
L1

Fig. 4



4 a, 4 b : Internal conductor
7 a, 7 b, 7 c, 7 d : Insulating material sheet
8 a, 8 b, 8 c, 8 d : Via hole

Fig. 5

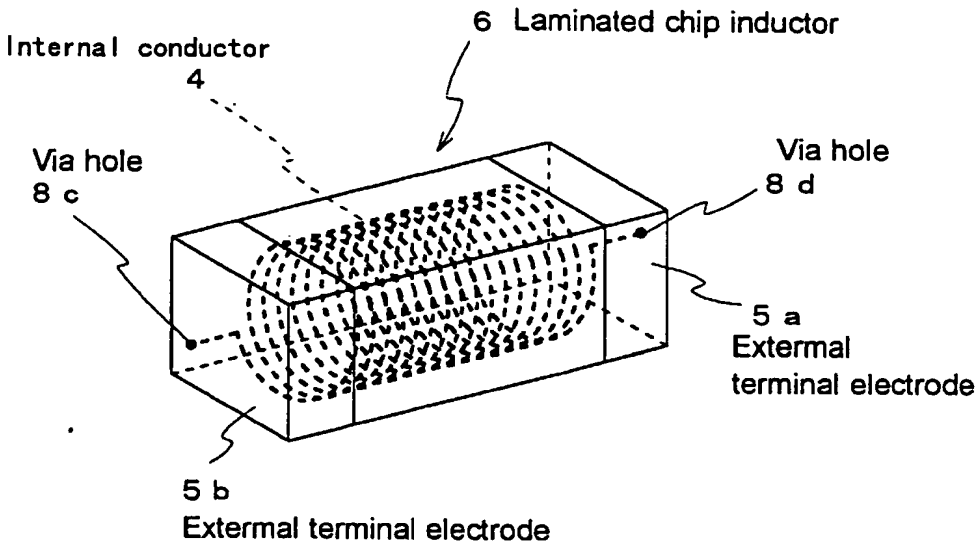

6 Laminated chip inductor
Internal conductor
4
Via hole
8 c
Via hole
8 d
5 a
Extermal
terminal electrode
5 b
Extermal terminal electrode

Fig. 6

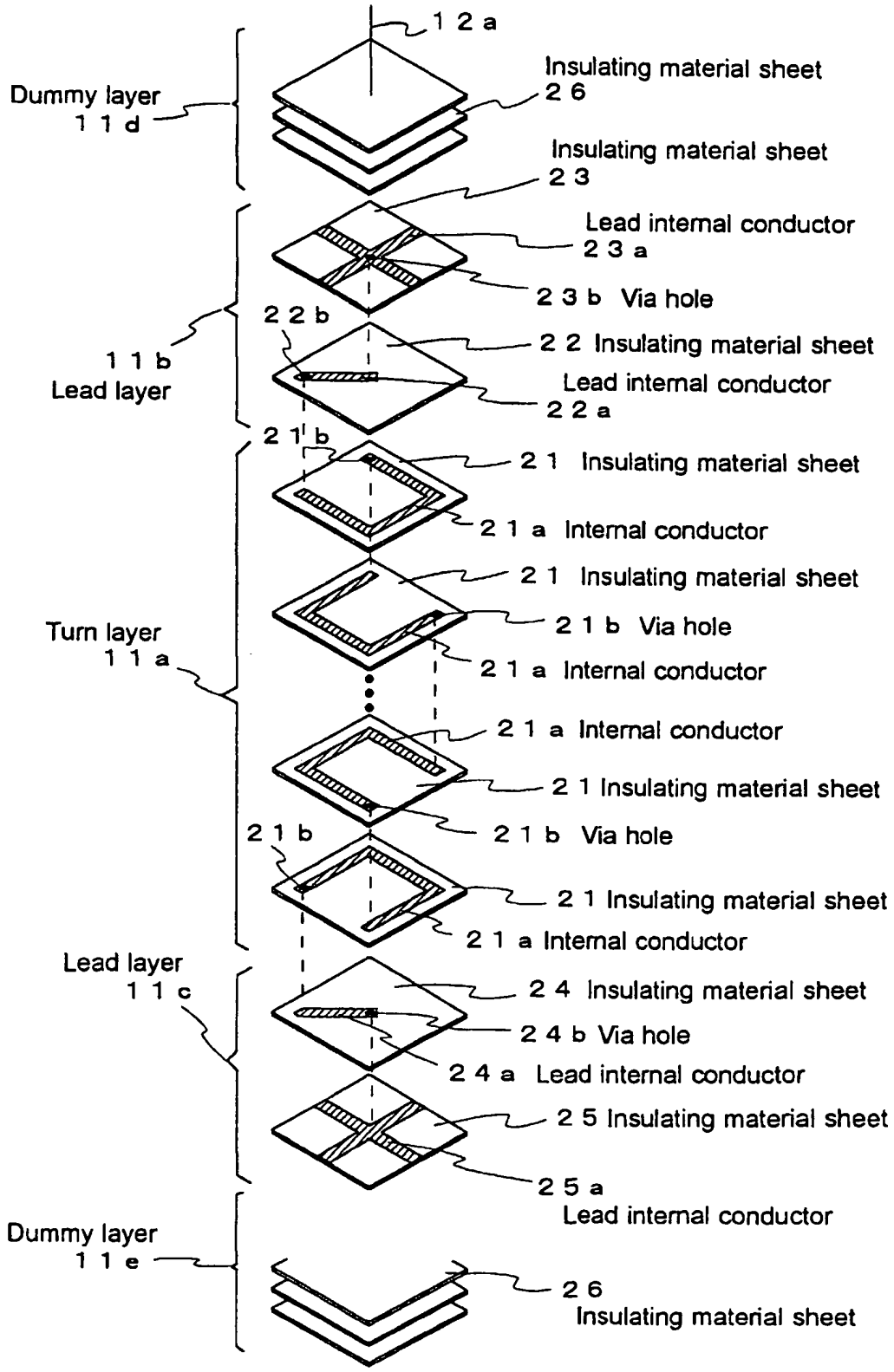

12a
Insulating material sheet
26
Dummy layer
11d
Insulating material sheet
23
Lead internal conductor
23a
23b Via hole
22b
22 Insulating material sheet
11b
Lead layer
Lead internal conductor
22a
21b
21 Insulating material sheet
21a Internal conductor
21 Insulating material sheet
Turn layer
11a
21b Via hole
21a Internal conductor
21a Internal conductor
21 Insulating material sheet
21b Via hole
21b
21 Insulating material sheet
21a Internal conductor
Lead layer
11c
24 Insulating material sheet
24b Via hole
24a Lead internal conductor
25 Insulating material sheet
25a
Lead internal conductor
Dummy layer
11e
26
Insulating material sheet

Fig. 7

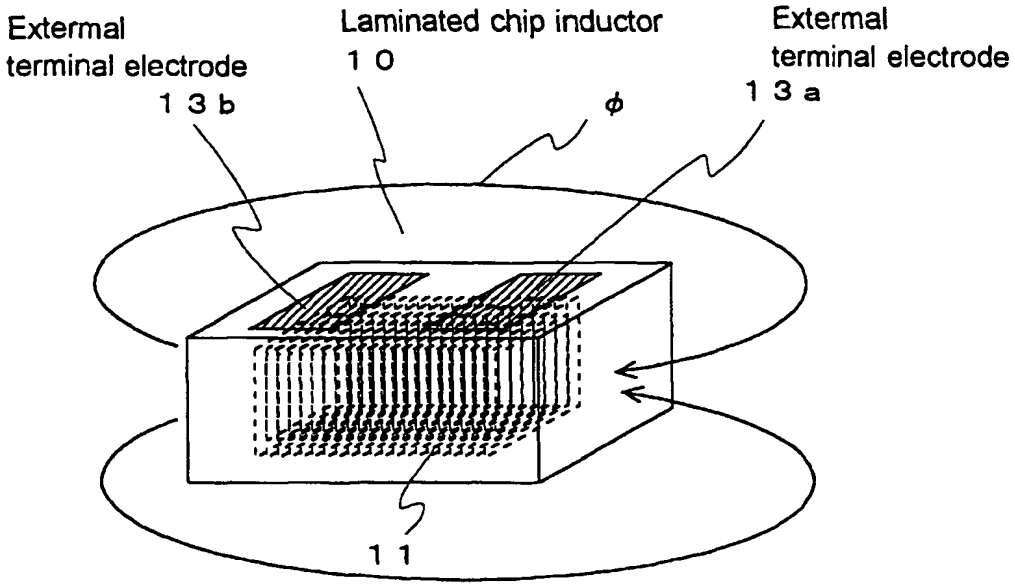

External
terminal electrode
13b
Laminated chip inductor
10
ϕ
External
terminal electrode
13a
11

Fig. 8 a

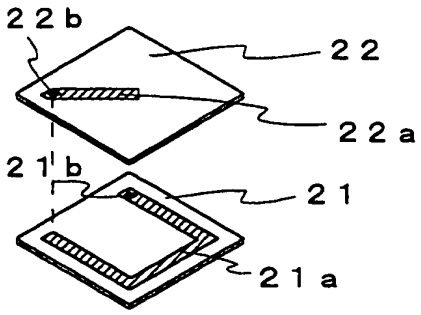


Fig. 8 b

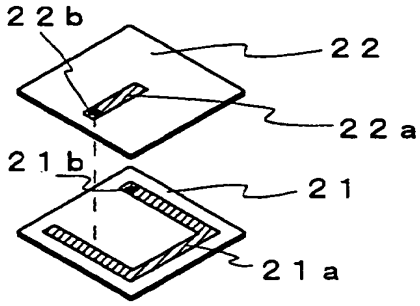


Fig. 8 c

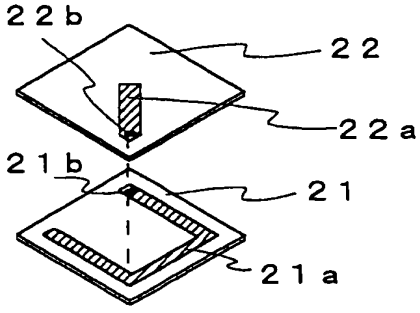


Fig. 8 d

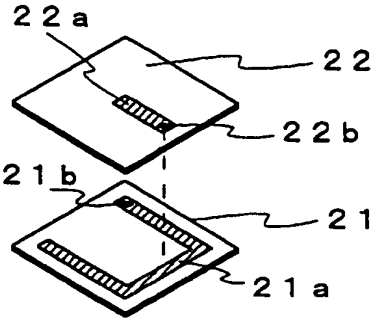


Fig. 8 e

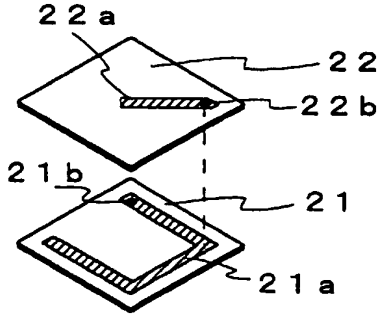


Fig. 8 f

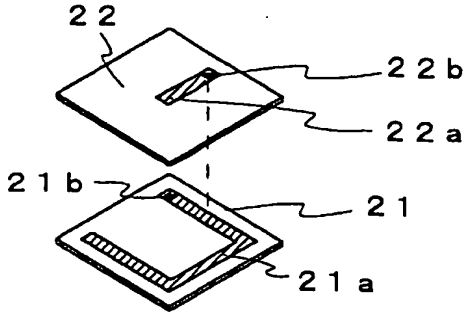


Fig. 8 g

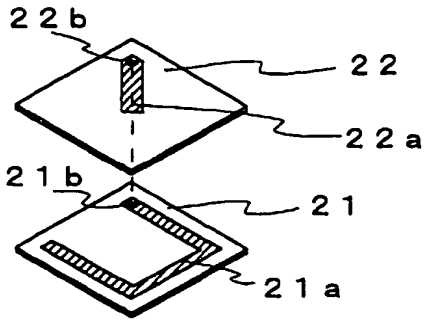

2 2 b
2 2
2 2 a
2 1 b
2 1
2 1 a

Fig. 9

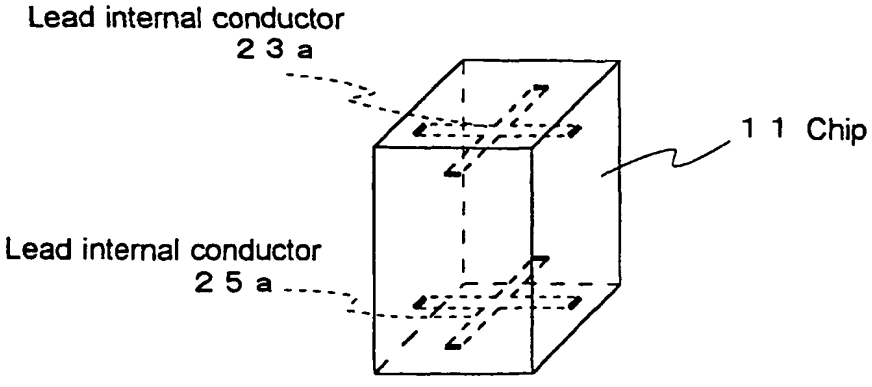

Lead internal conductor
2 3 a
1 1 Chip
Lead internal conductor
2 5 a

Fig. 10

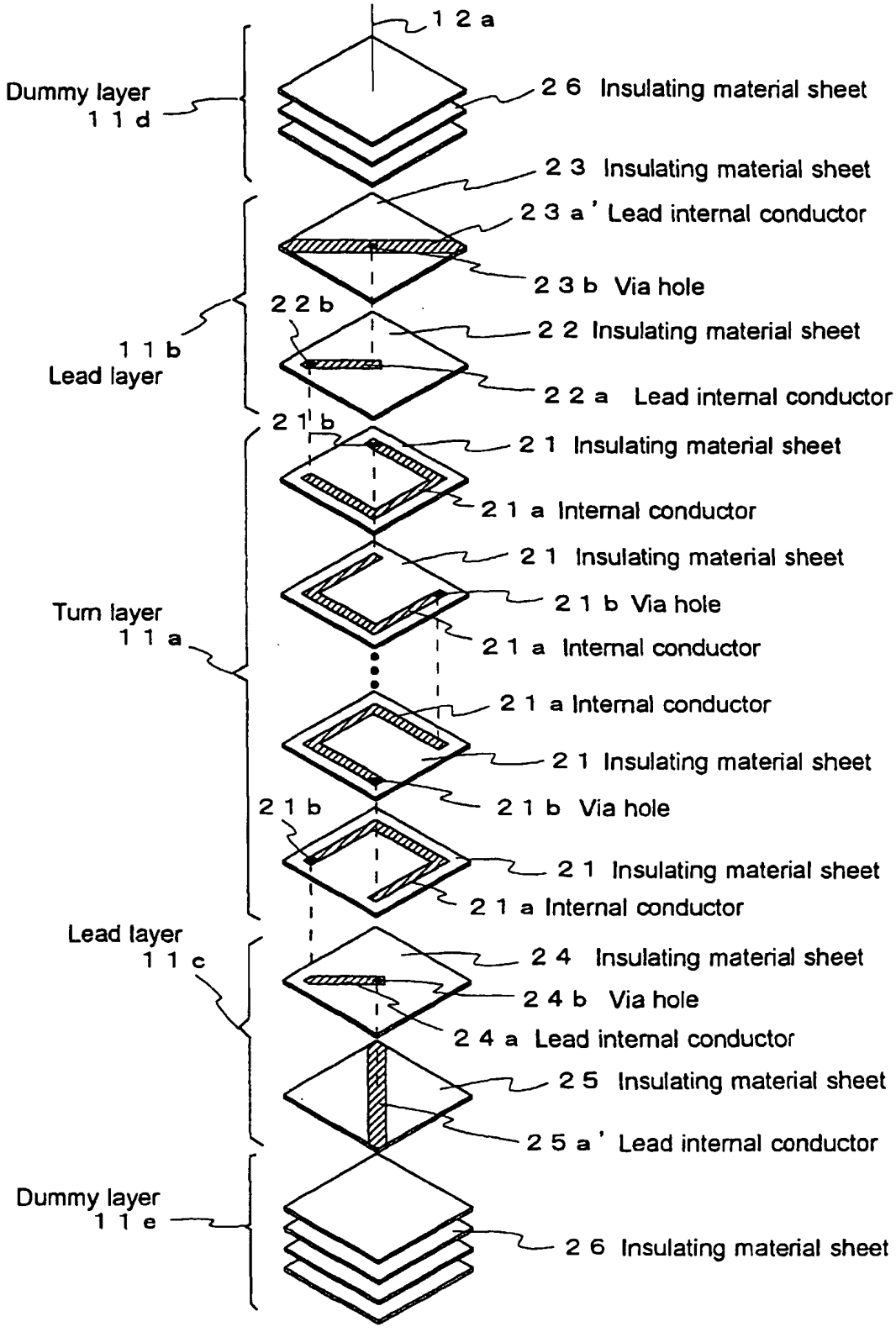

12a
Dummy layer
11d
26 Insulating material sheet
23 Insulating material sheet
23a' Lead internal conductor
23b Via hole
22b
22 Insulating material sheet
11b
Lead layer
22a Lead internal conductor
21b
21 Insulating material sheet
21a Internal conductor
21 Insulating material sheet
Tum layer
11a
21b Via hole
21a Internal conductor
21a Internal conductor
21 Insulating material sheet
21b Via hole
21b
21 Insulating material sheet
21a Internal conductor
Lead layer
11c
24 Insulating material sheet
24b Via hole
24a Lead internal conductor
25 Insulating material sheet
25a' Lead internal conductor
Dummy layer
11e
26 Insulating material sheet

Fig. 1 1

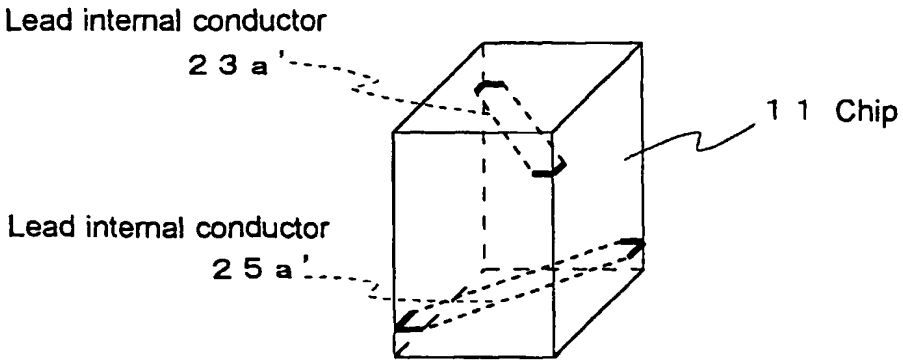

Lead internal conductor
2 3 a '
1 1 Chip
Lead internal conductor
2 5 a '

Fig. 12

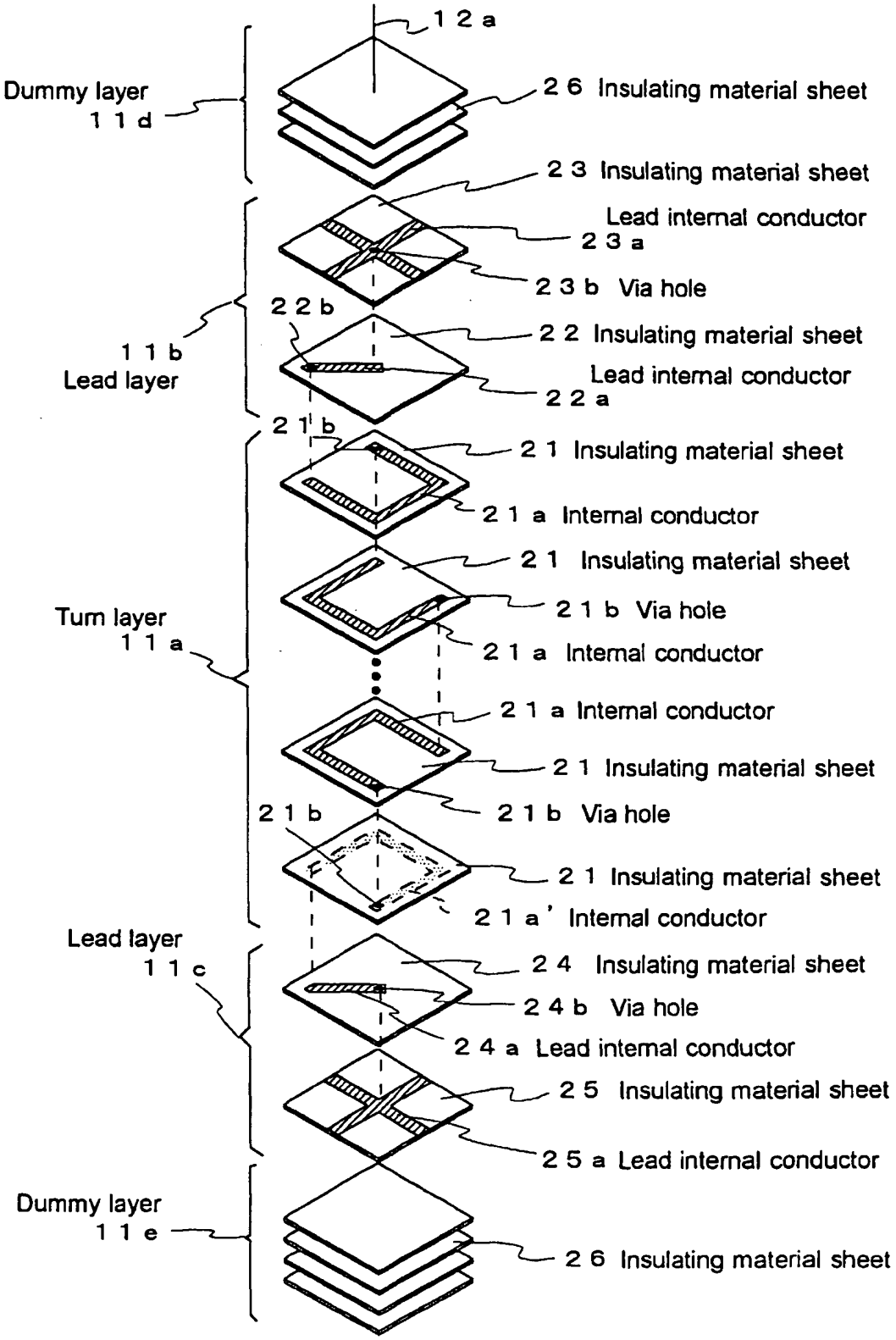

12a
Dummy layer
11d
26 Insulating material sheet
23 Insulating material sheet
Lead internal conductor
23a
23b Via hole
22b
11b
Lead layer
22 Insulating material sheet
Lead internal conductor
22a
21b
21 Insulating material sheet
21a Internal conductor
21 Insulating material sheet
Turn layer
11a
21b Via hole
21a Internal conductor
21a Internal conductor
21 Insulating material sheet
21b Via hole
21b
21 Insulating material sheet
21a' Internal conductor
Lead layer
11c
24 Insulating material sheet
24b Via hole
24a Lead internal conductor
25 Insulating material sheet
25a Lead internal conductor
Dummy layer
11e
26 Insulating material sheet

Fig. 1 3 a

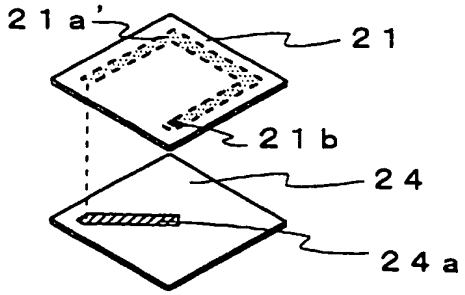


Fig. 1 3 b

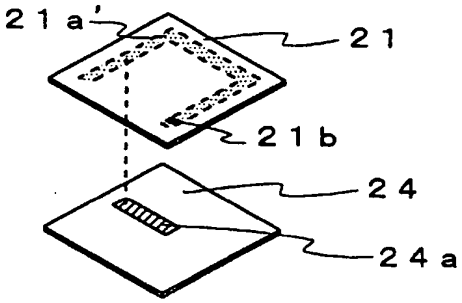


Fig. 1 3 c

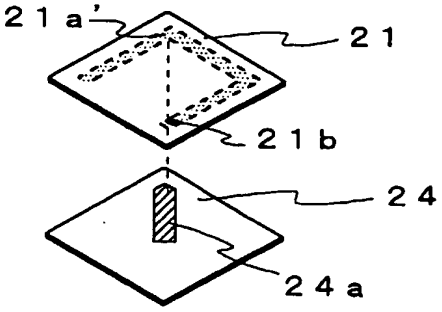


Fig. 1 3 d

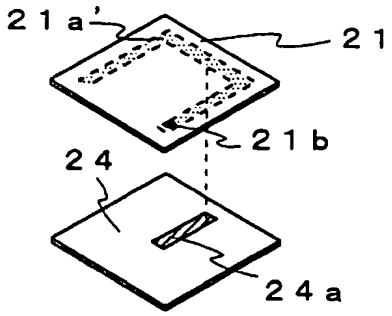


Fig. 1 3 e

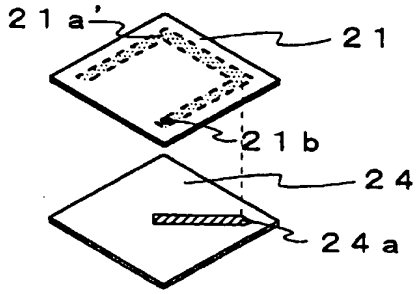


Fig. 1 3 f

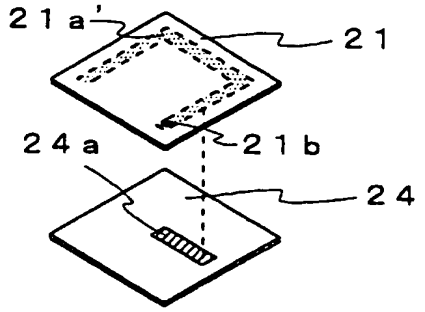


Fig. 1 3 g

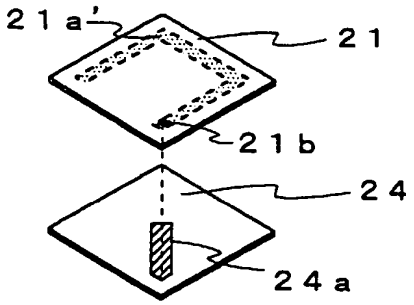


Fig. 1 4

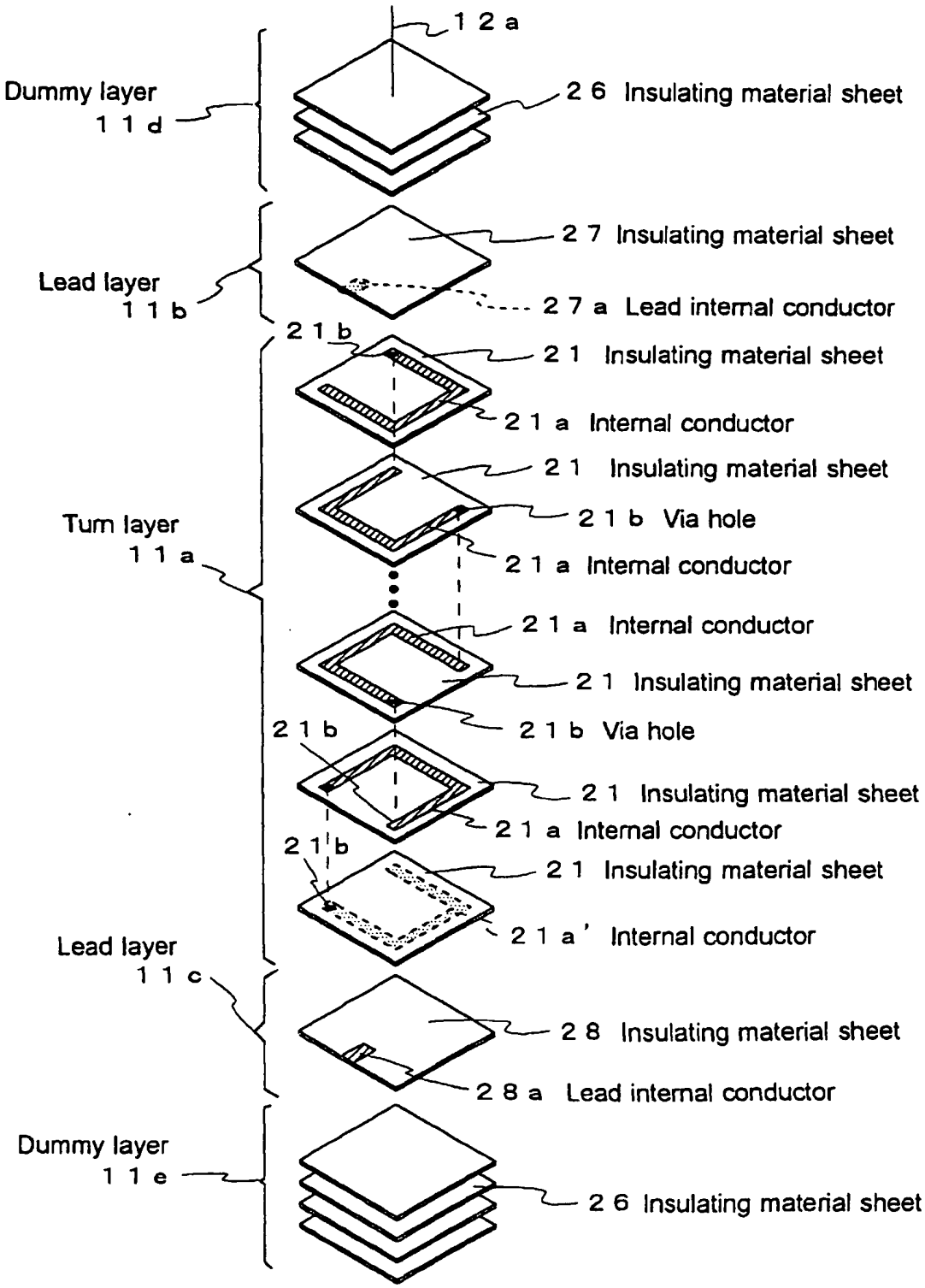

12a
Dummy layer
11d
26 Insulating material sheet
27 Insulating material sheet
Lead layer
11b
27a Lead internal conductor
21b
21 Insulating material sheet
21a Internal conductor
21 Insulating material sheet
Tum layer
11a
21b Via hole
21a Internal conductor
21a Internal conductor
21 Insulating material sheet
21b
21b Via hole
21 Insulating material sheet
21a Internal conductor
21b
21 Insulating material sheet
21a' Internal conductor
Lead layer
11c
28 Insulating material sheet
28a Lead internal conductor
Dummy layer
11e
26 Insulating material sheet

Fig. 15

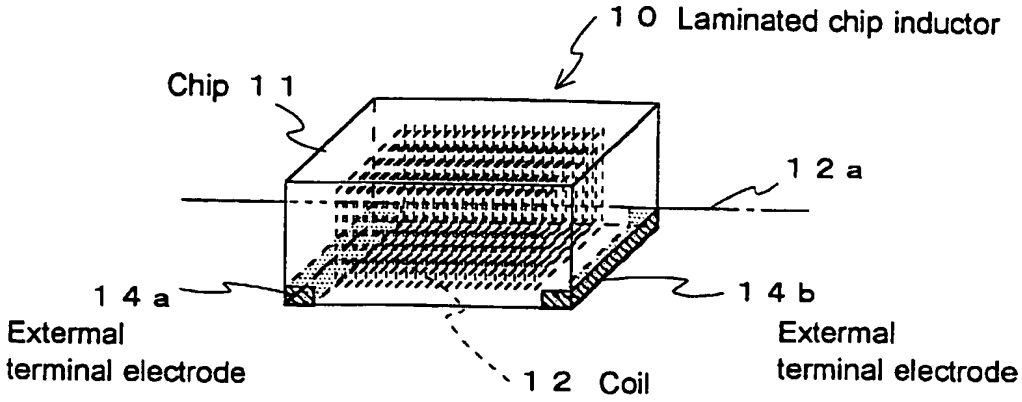

10 Laminated chip inductor
Chip 11
12a
14a
External terminal electrode
14b
External terminal electrode
12 Coil

Fig. 16

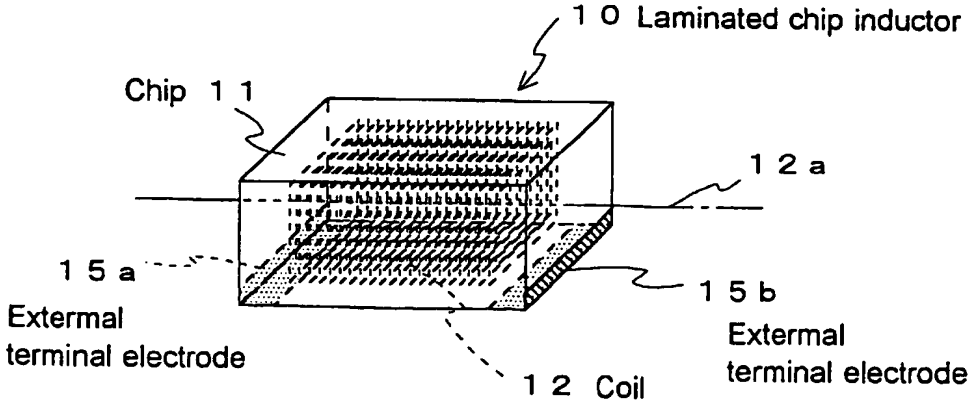

10 Laminated chip inductor
Chip 11
12a
15a
External terminal electrode
15b
External terminal electrode
12 Coil

Fig. 17

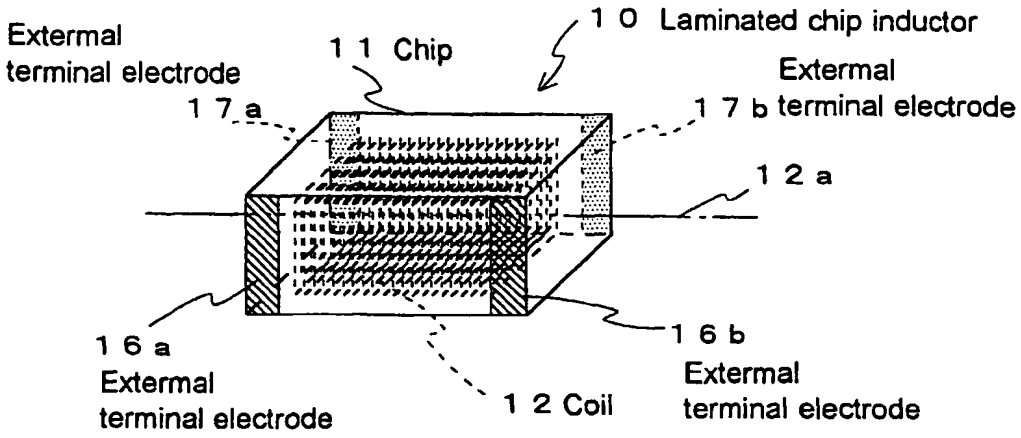

External
terminal electrode
17a
11 Chip
10 Laminated chip inductor
External
17b terminal electrode
12a
16a
External
terminal electrode
12 Coil
16b
External
terminal electrode

Fig. 18

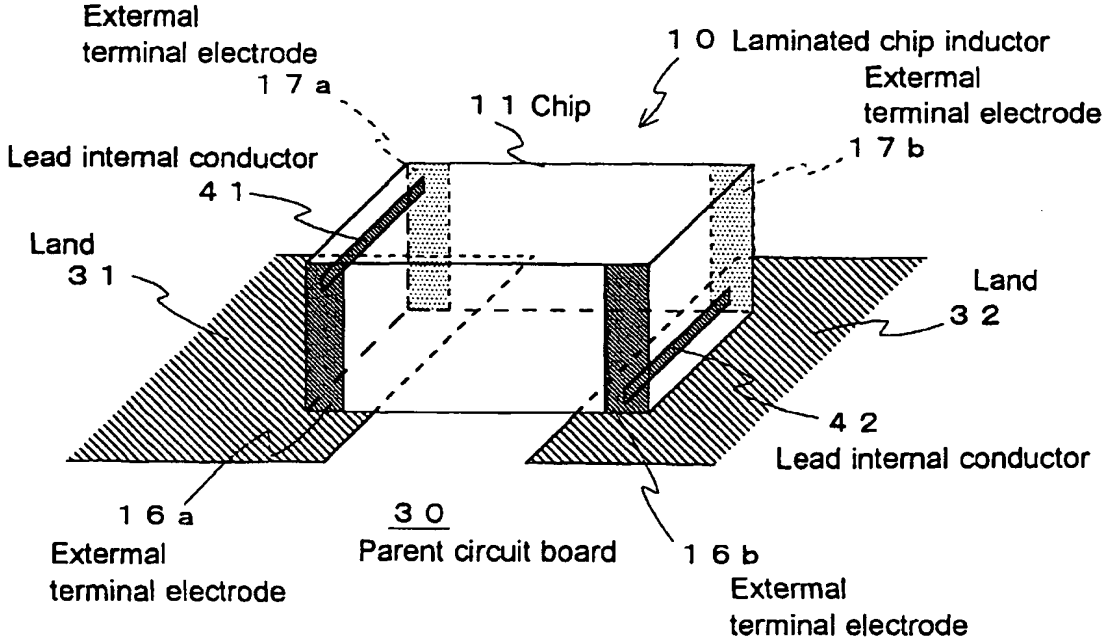

External
terminal electrode
17a
10 Laminated chip inductor
11 Chip
External
terminal electrode
17b
Lead internal conductor
41
Land
31
Land
32
42
Lead internal conductor
16a
External
terminal electrode
30
Parent circuit board
16b
External
terminal electrode

Fig. 19

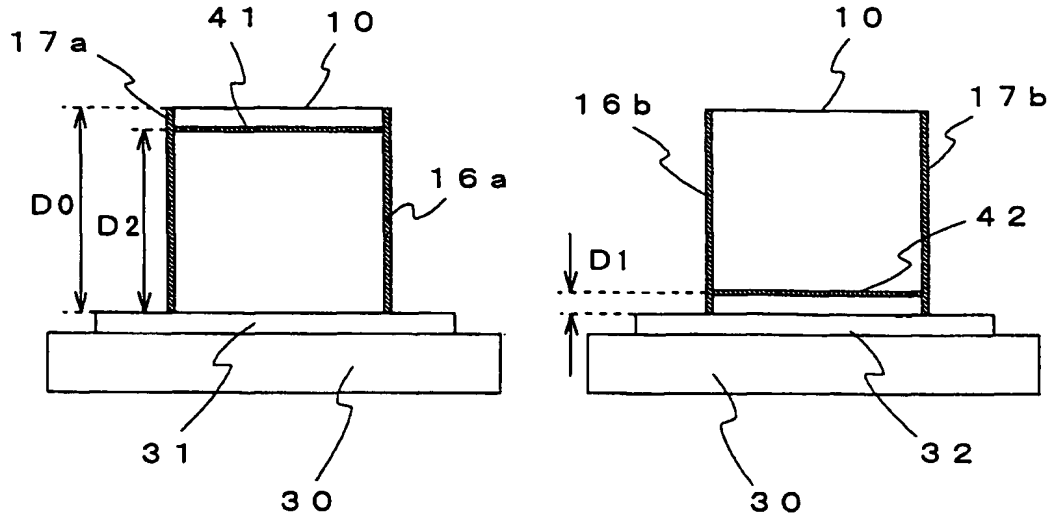

17a
41
10
D0
D2
16a
31
30
10
16b
17b
42
D1
32
30

Fig. 20

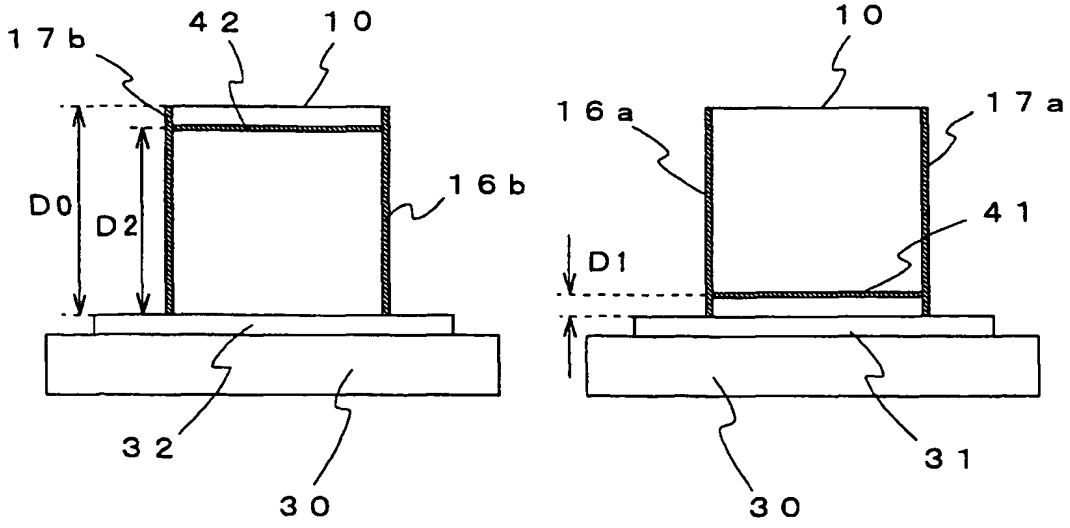

17b
42
10
D0
D2
16b
32
30
10
16a
17a
41
D1
31
30

Fig. 2 1

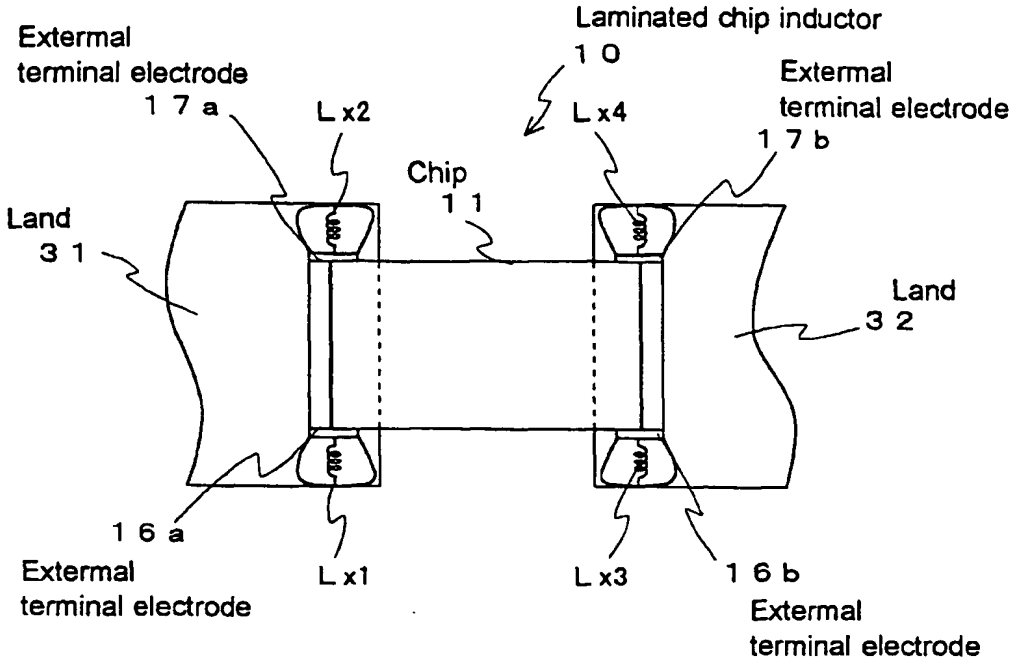

External terminal electrode
17a
Lx2
Laminated chip inductor
10
Lx4
External terminal electrode
17b
Chip
11
Land
31
Land
32
16a
External terminal electrode
Lx1
Lx3
16b
External terminal electrode

Fig. 2 2

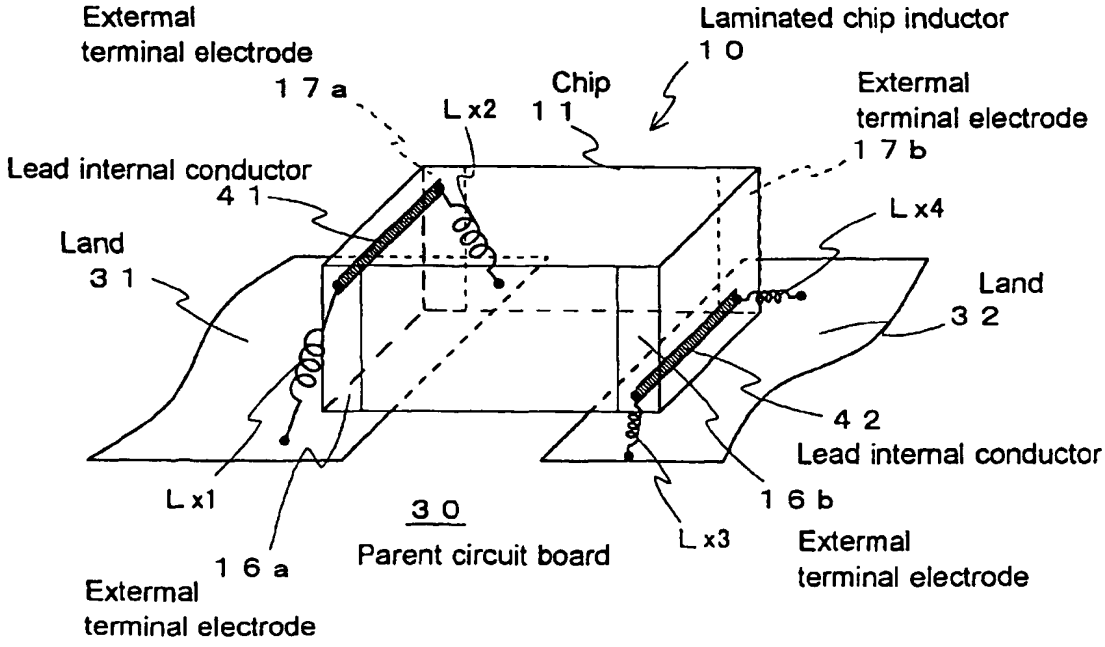

External terminal electrode
17a
Lx2
Chip
11
Laminated chip inductor
10
External terminal electrode
17b
Lead internal conductor
41
Lx4
Land
31
Land
32
42
Lead internal conductor
Lx1
30
Parent circuit board
16b
Lx3
External terminal electrode
16a
External terminal electrode

Fig. 23

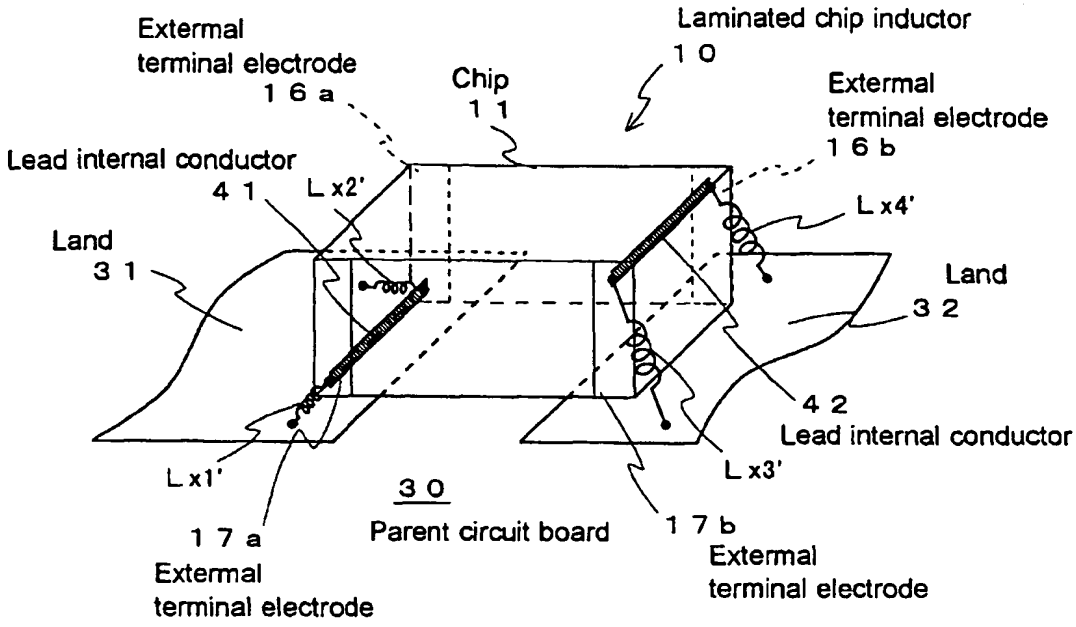

External terminal electrode 16a
Chip 11
Laminated chip inductor 10
External terminal electrode 16b
Lead internal conductor 41
Lx2'
Lx4'
Land 31
Land 32
42 Lead internal conductor
Lx1'
Lx3'
30 Parent circuit board
17a External terminal electrode
17b External terminal electrode

Fig. 24

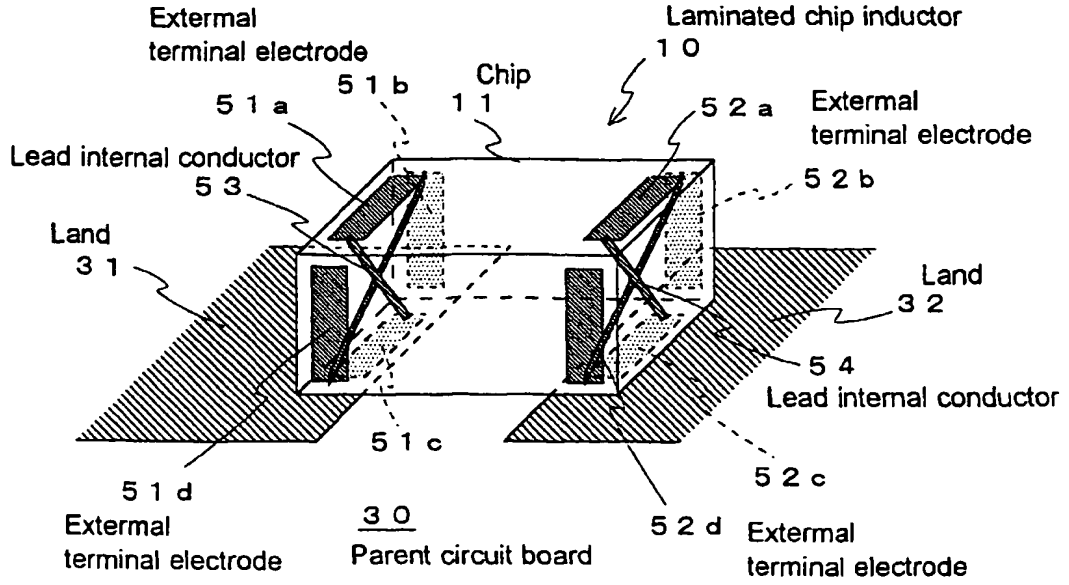

External terminal electrode
51b
51a
Chip 11
Laminated chip inductor 10
52a
External terminal electrode
Lead internal conductor 53
52b
Land 31
Land 32
54 Lead internal conductor
51c
52c
51d External terminal electrode
30 Parent circuit board
52d External terminal electrode

Fig. 25

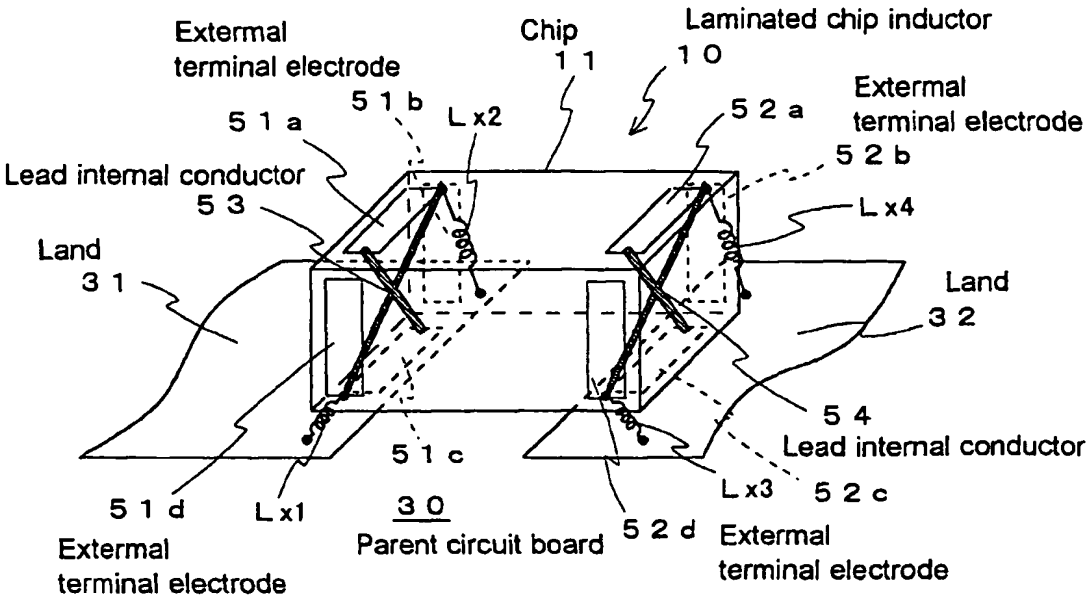

External terminal electrode
Chip 11
Laminated chip inductor 10
51b
51a
Lx2
52a
External terminal electrode
52b
Lead internal conductor 53
Lx4
Land 31
Land 32
54
Lead internal conductor
51c
Lx3
52c
51d
Lx1
30
Parent circuit board
52d
External terminal electrode
External terminal electrode

Fig. 26

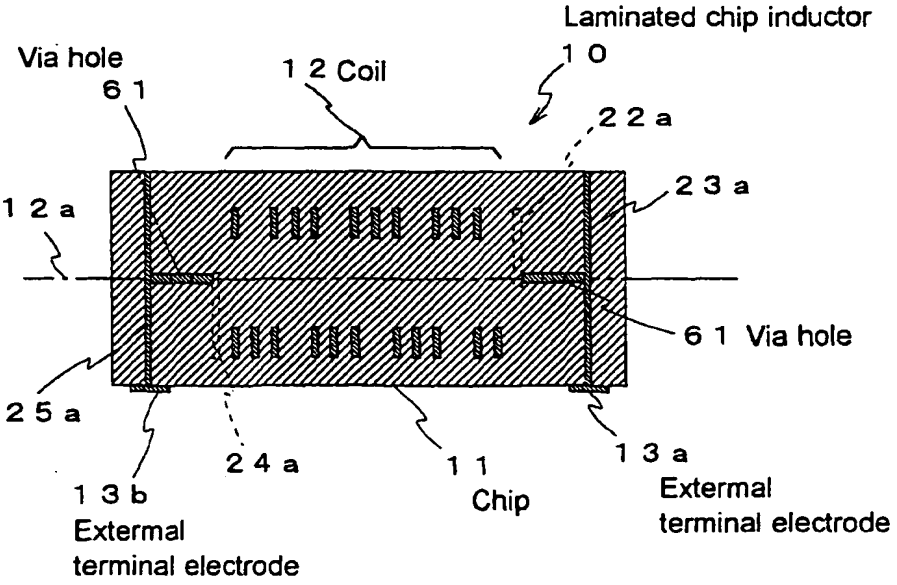

Laminated chip inductor
Via hole 61
12 Coil
10
22a
23a
12a
61 Via hole
25a
24a
11 Chip
13a External terminal electrode
13b External terminal electrode

Fig. 27

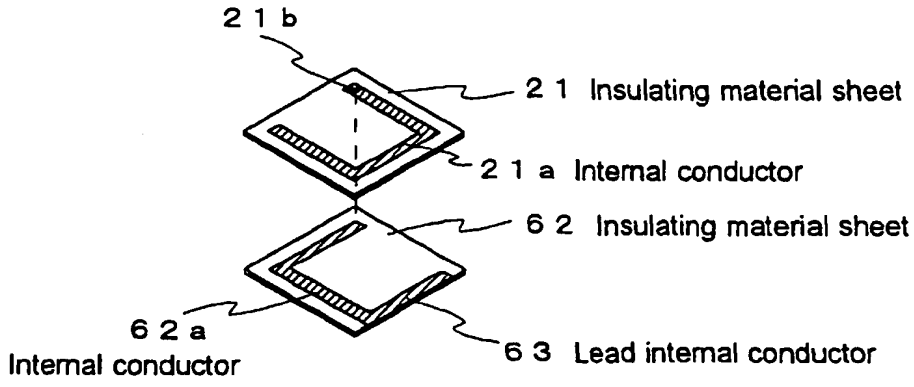

21b
21 Insulating material sheet
21a Internal conductor
62 Insulating material sheet
62a
Internal conductor
63 Lead internal conductor

Fig. 28

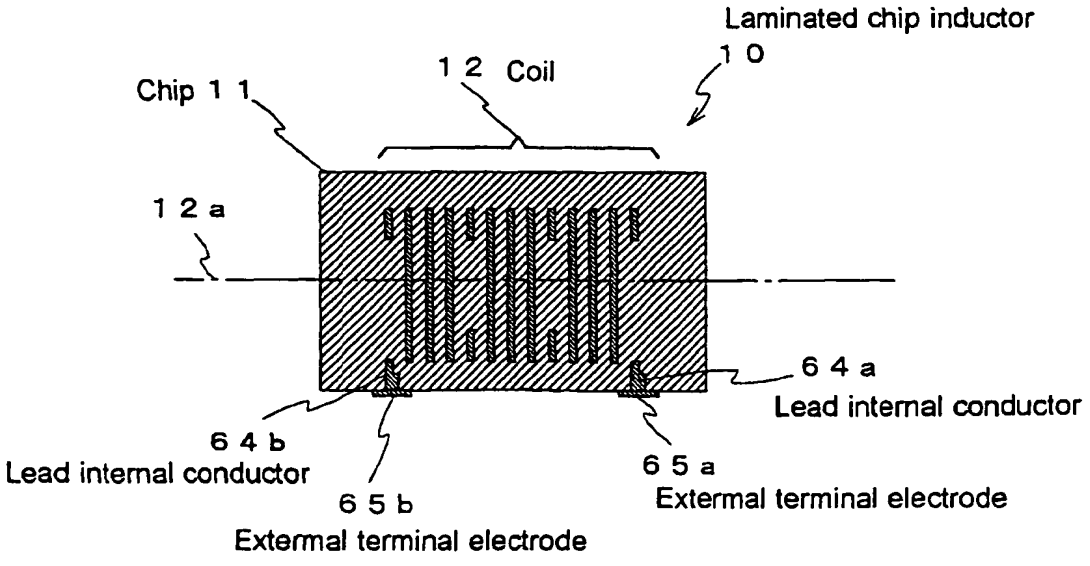
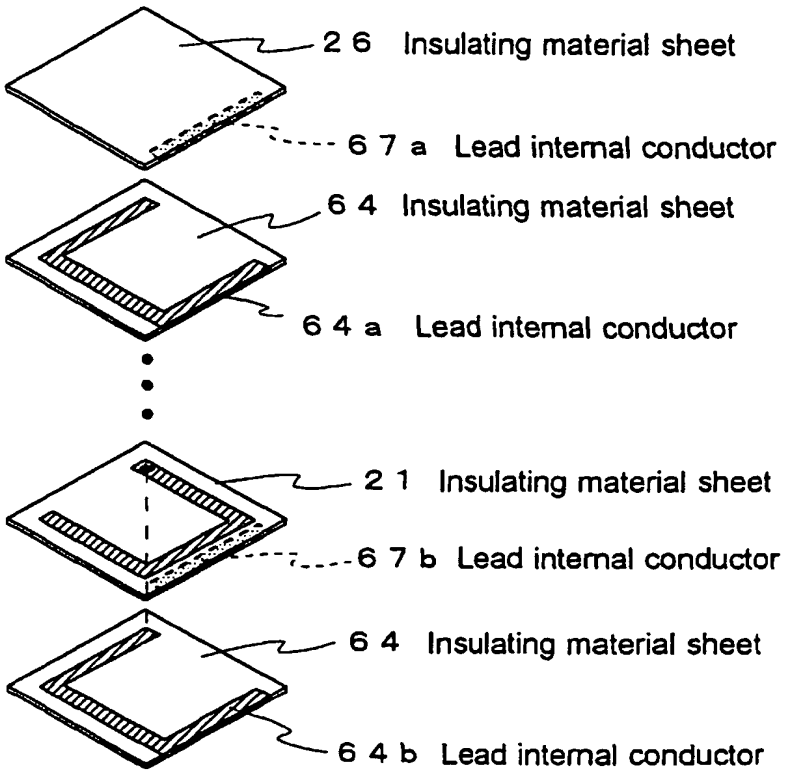

Laminated chip inductor
10
12 Coil
Chip 11
12a
64a
Lead internal conductor
64b
Lead internal conductor
65b
External terminal electrode
65a
External terminal electrode

Fig. 2 9


2 6 Insulating material sheet
6 7 a Lead internal conductor
6 4 Insulating material sheet
6 4 a Lead internal conductor
2 1 Insulating material sheet
6 7 b Lead internal conductor
6 4 Insulating material sheet
6 4 b Lead internal conductor